

FIG. 1

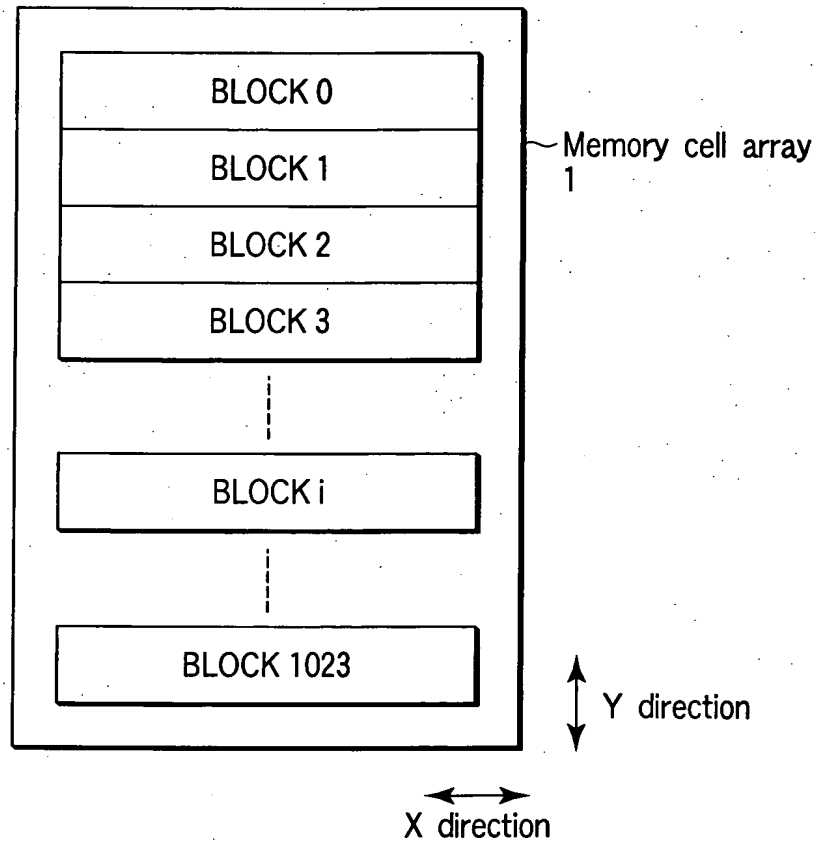
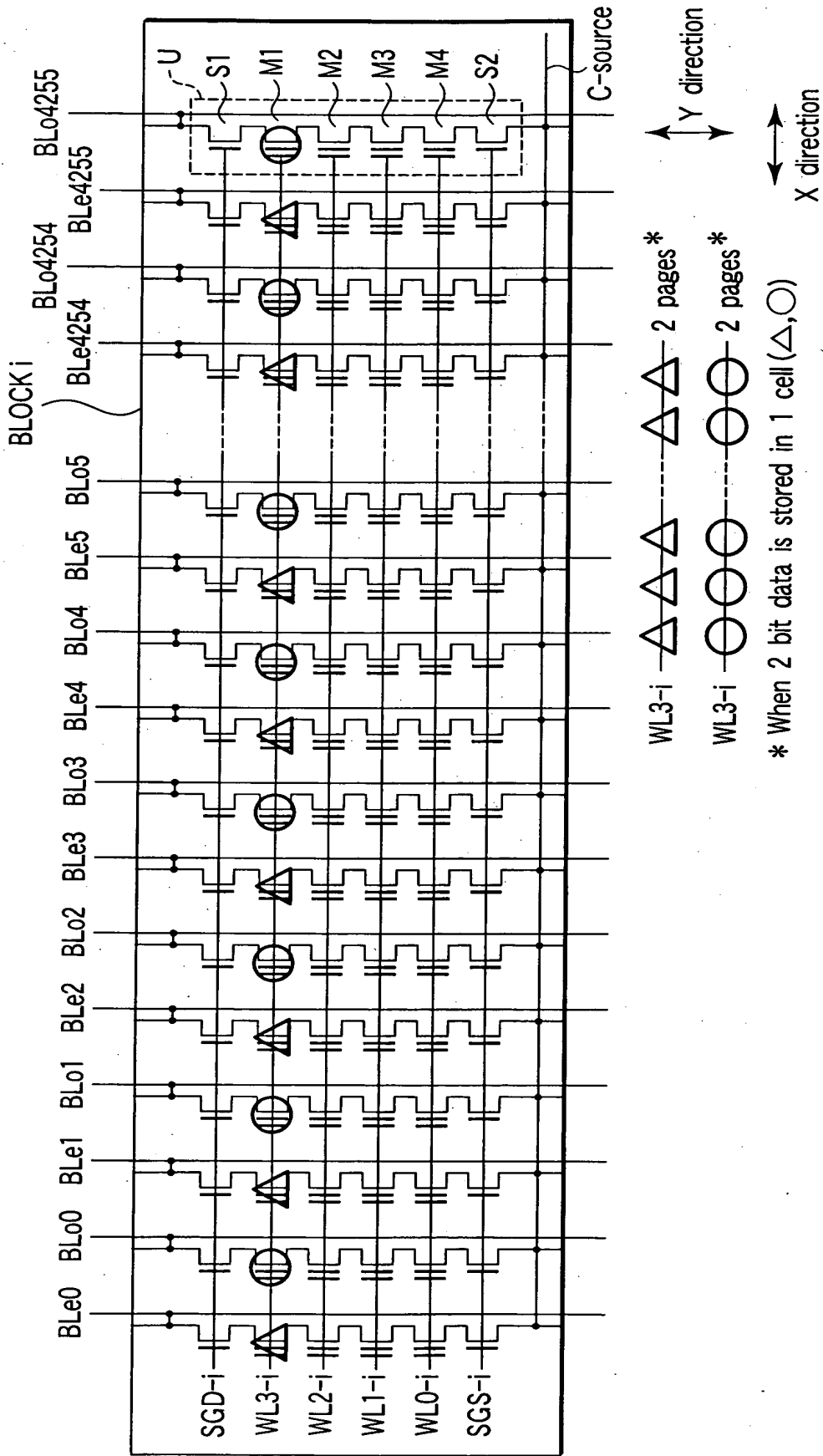


FIG. 2



### FIG. 3

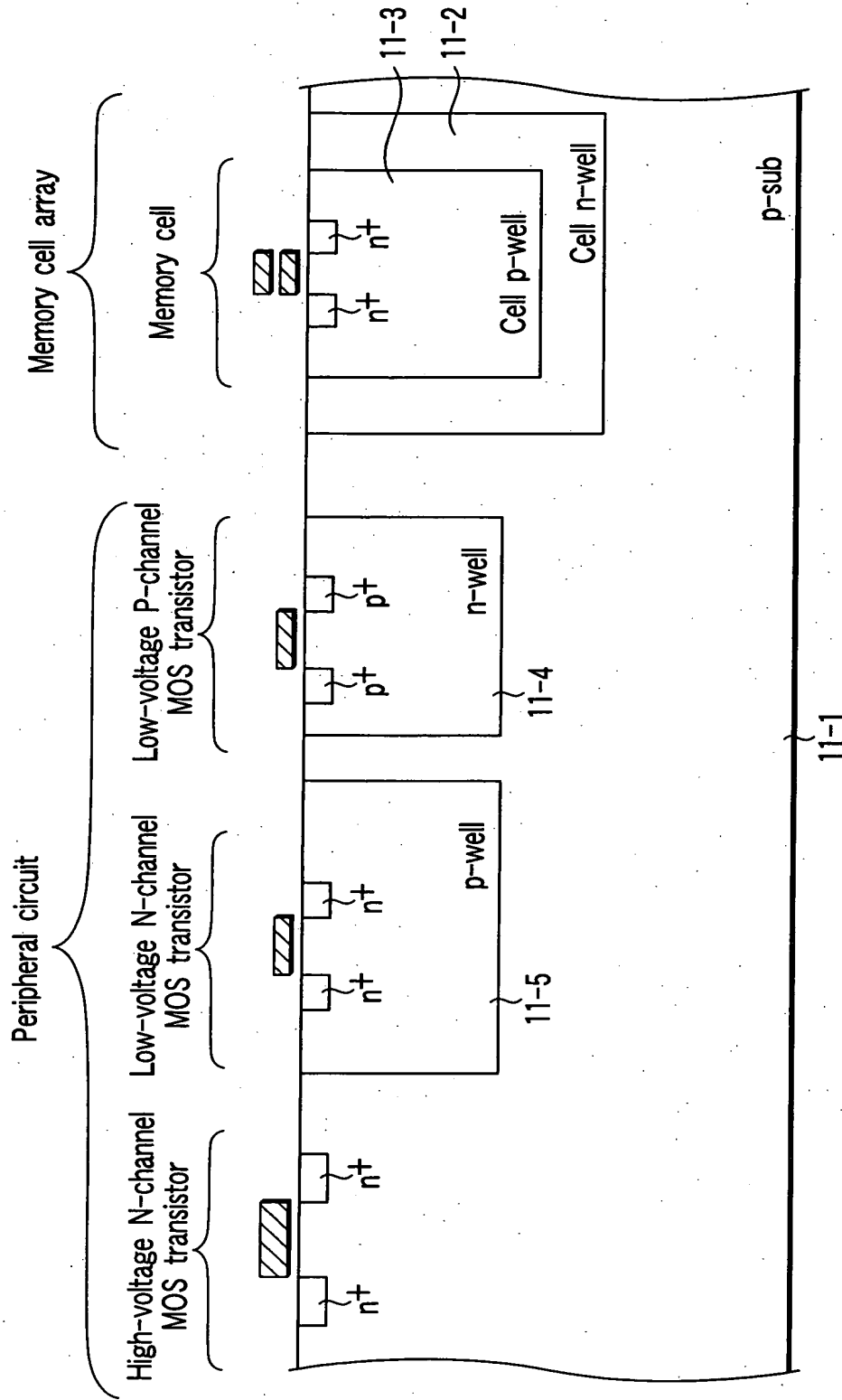


FIG. 4

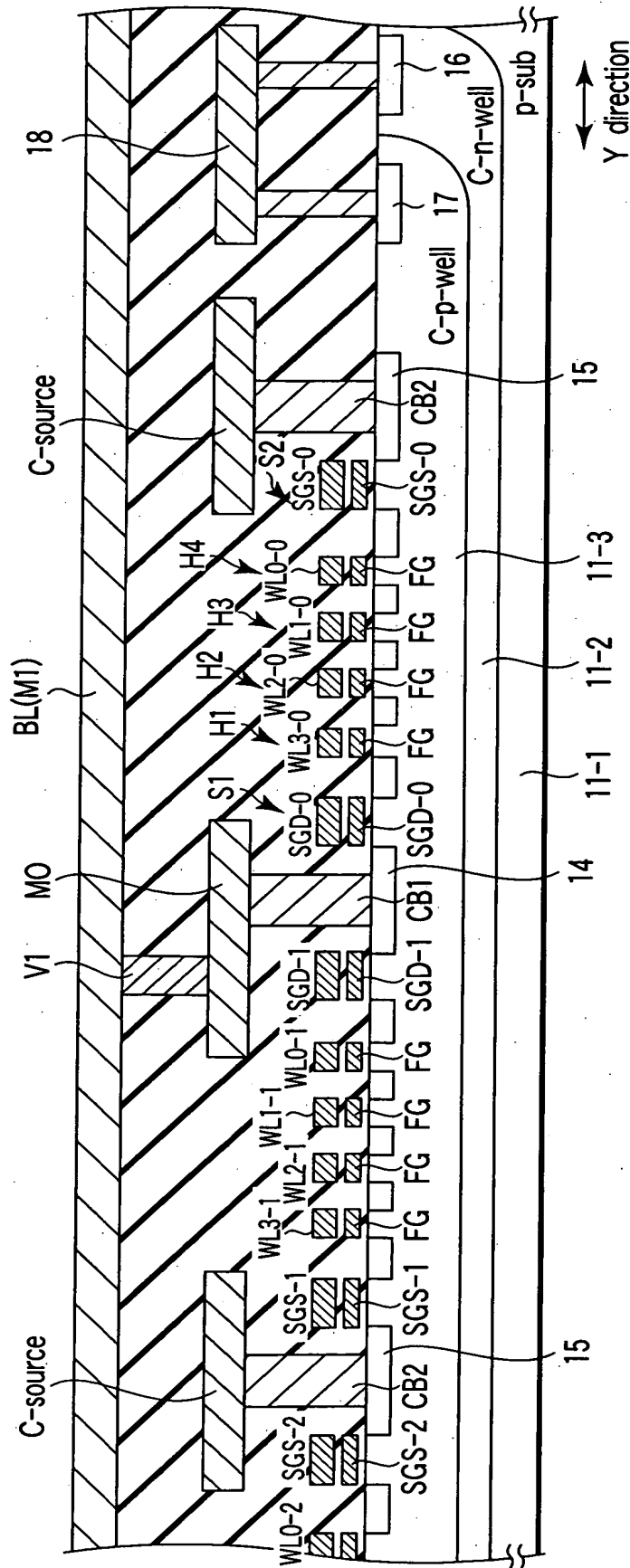


FIG. 5

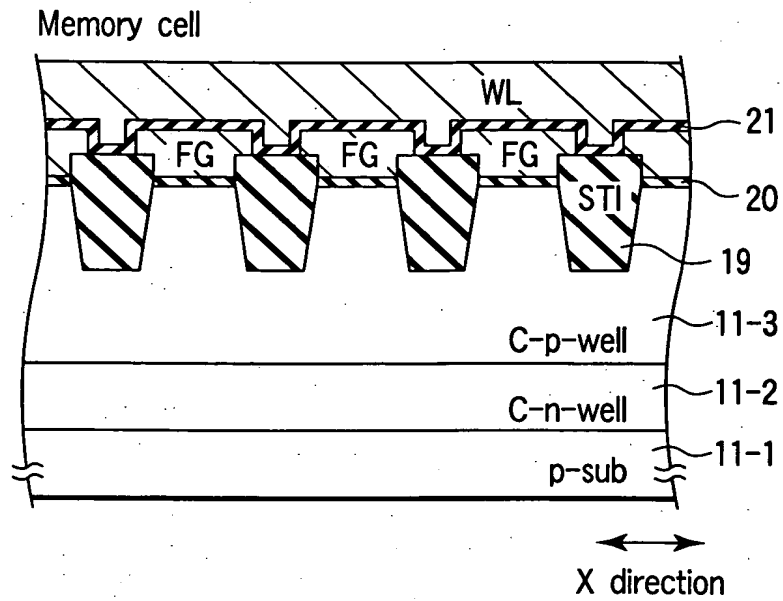


FIG. 6

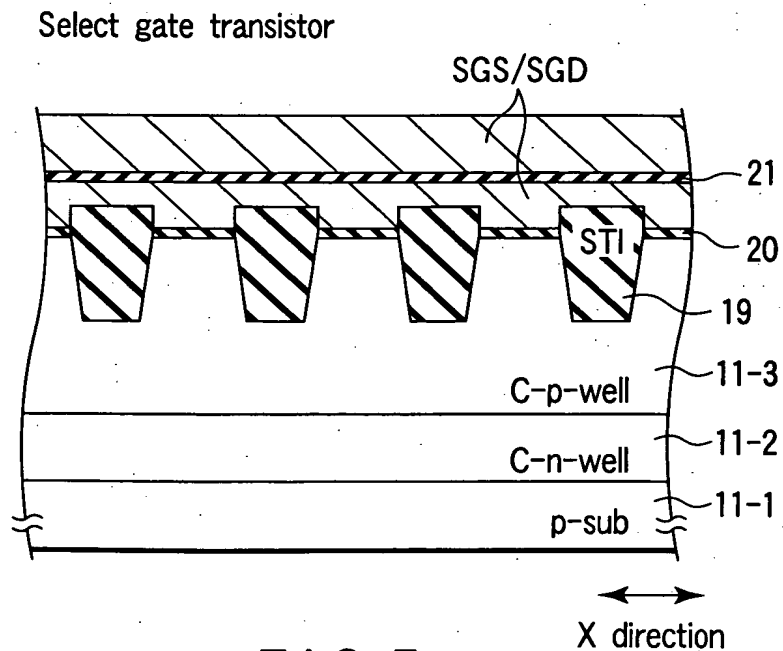


FIG. 7

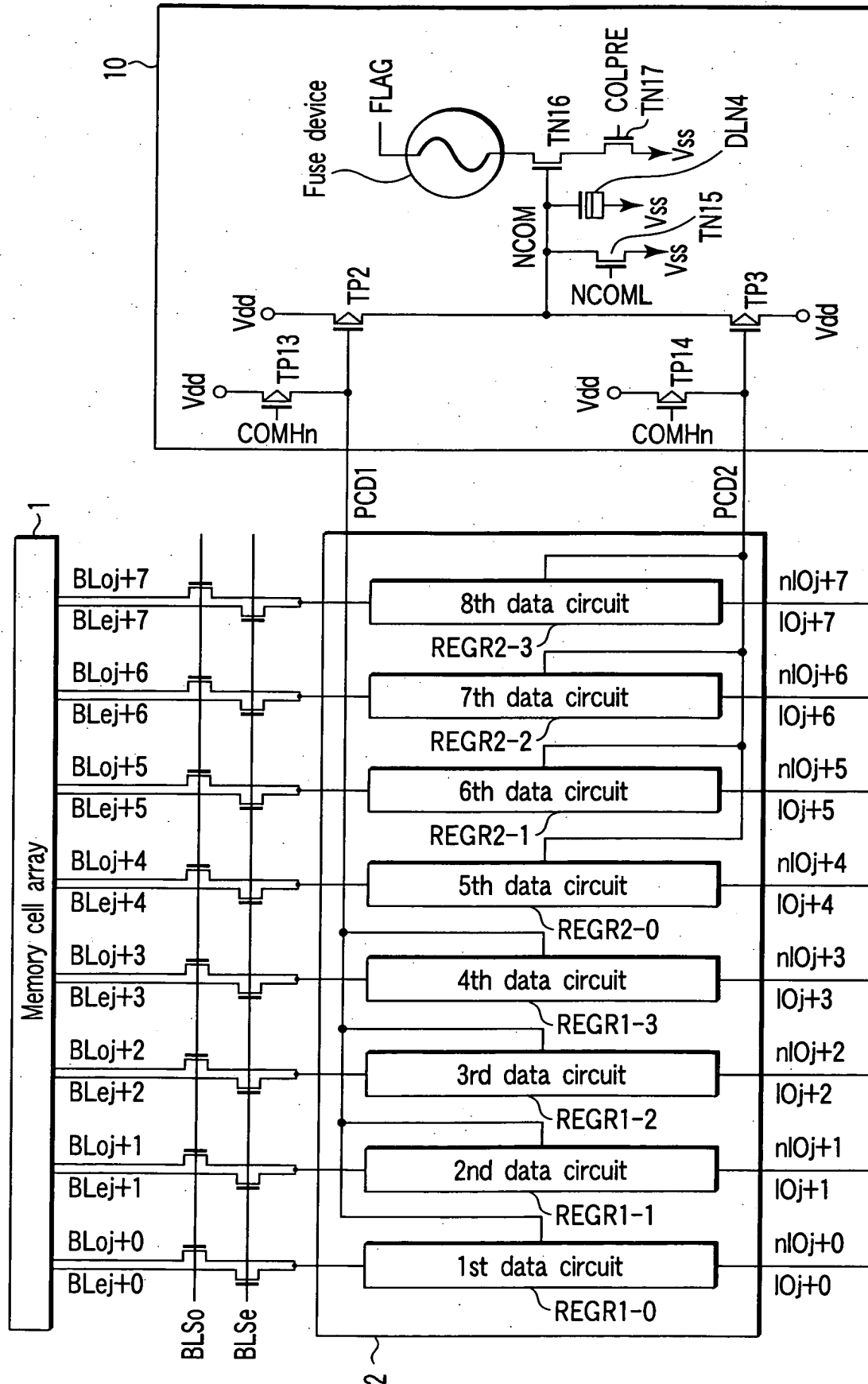


FIG.8

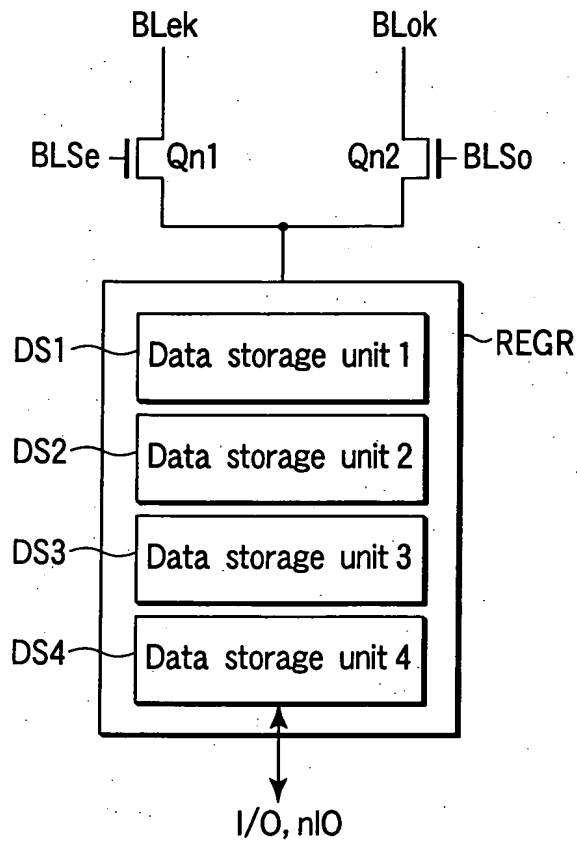


FIG. 9

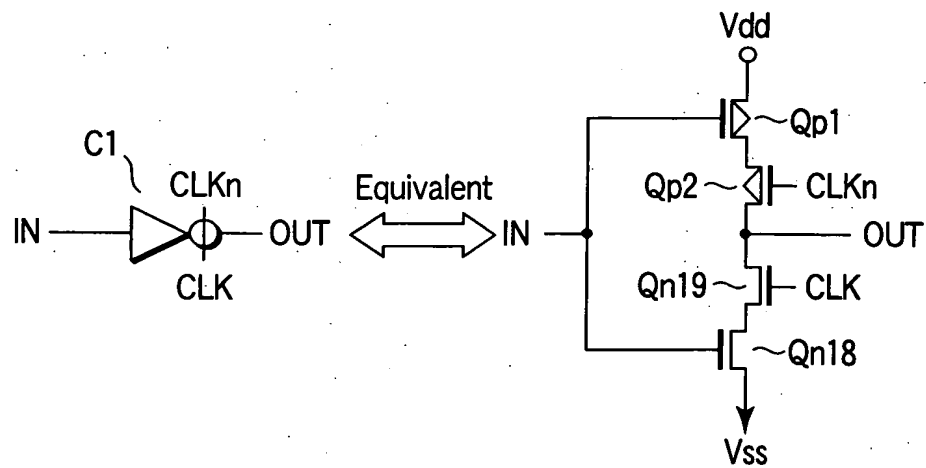


FIG. 11





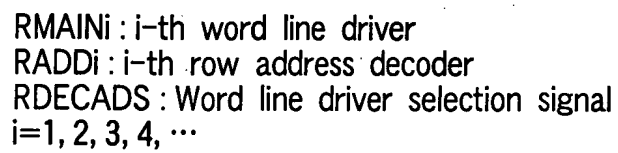


FIG. 12

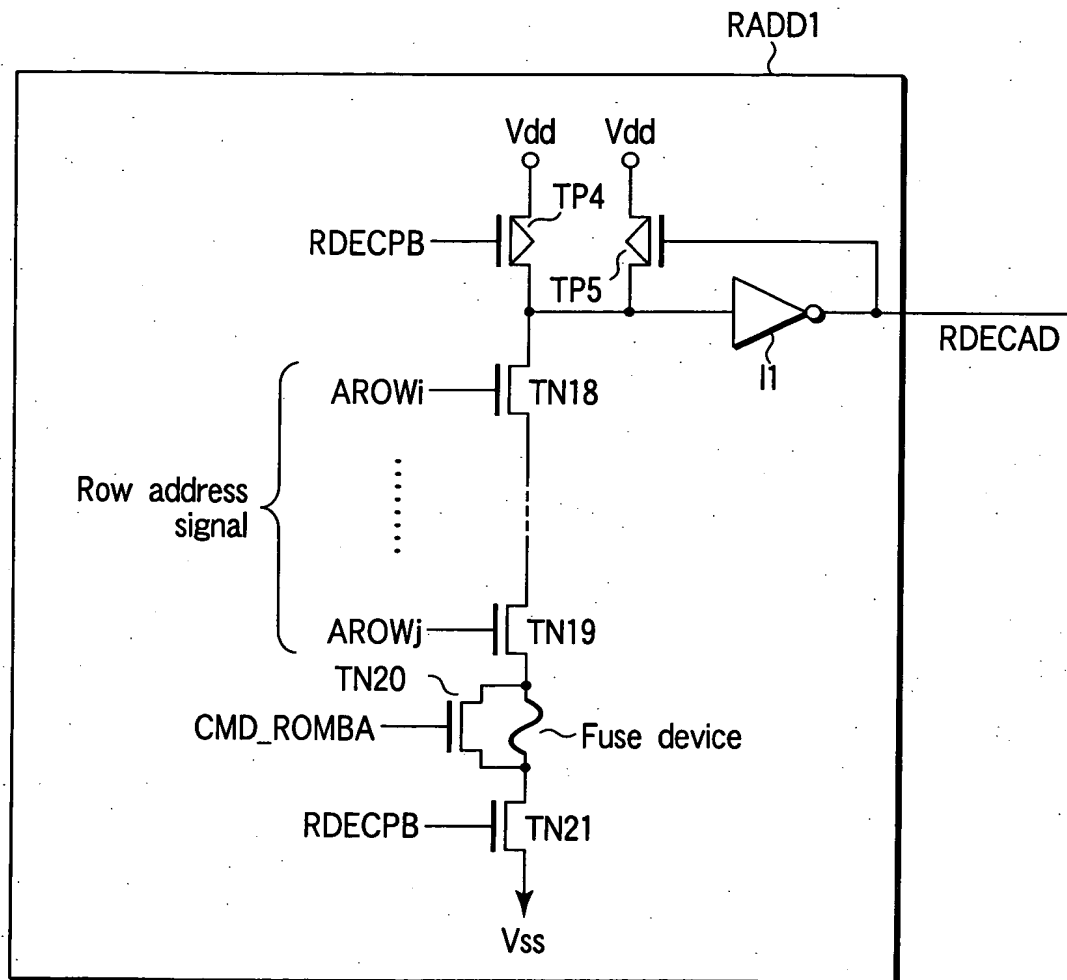


FIG. 13

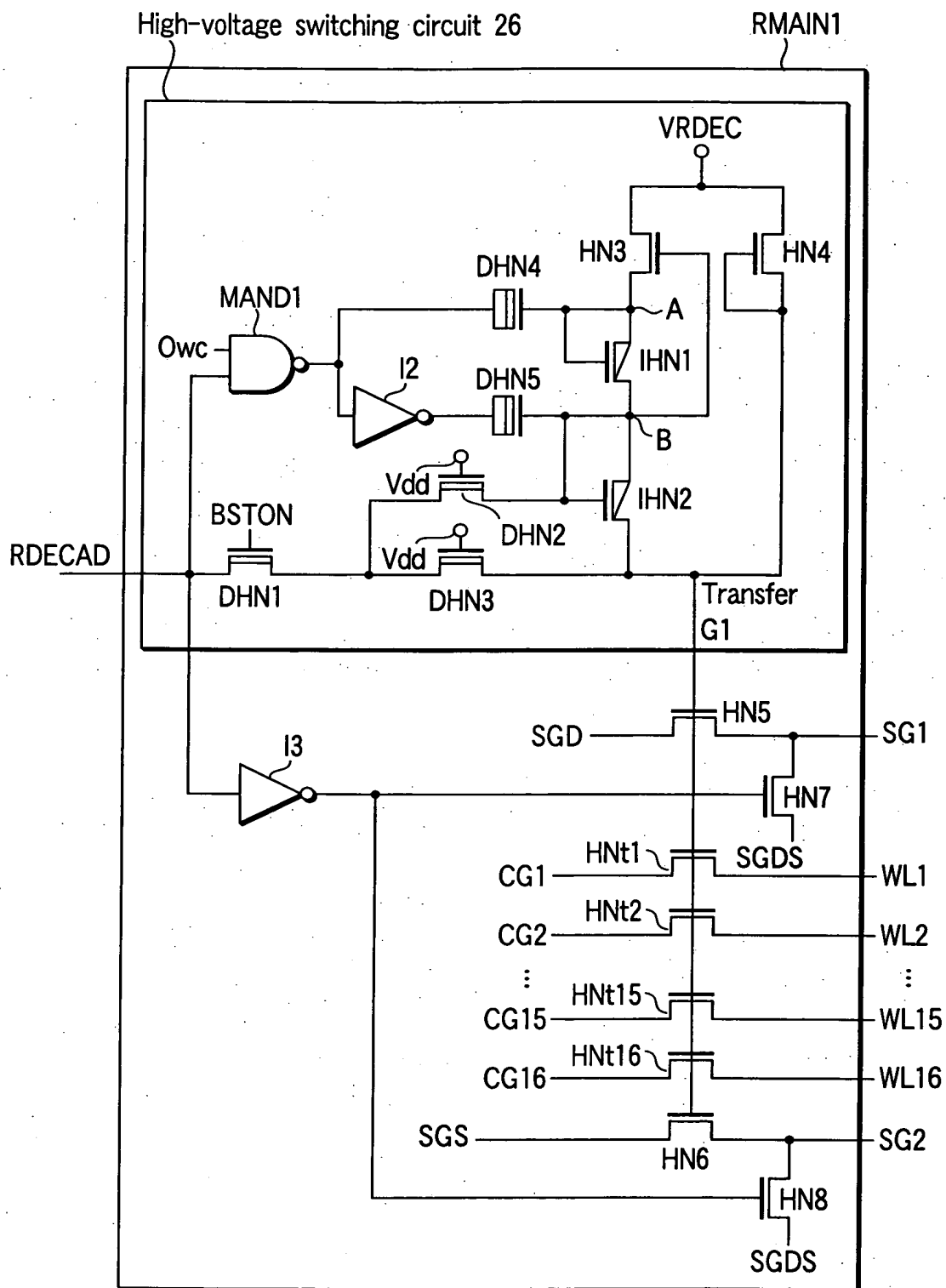


FIG. 14



FIG. 15

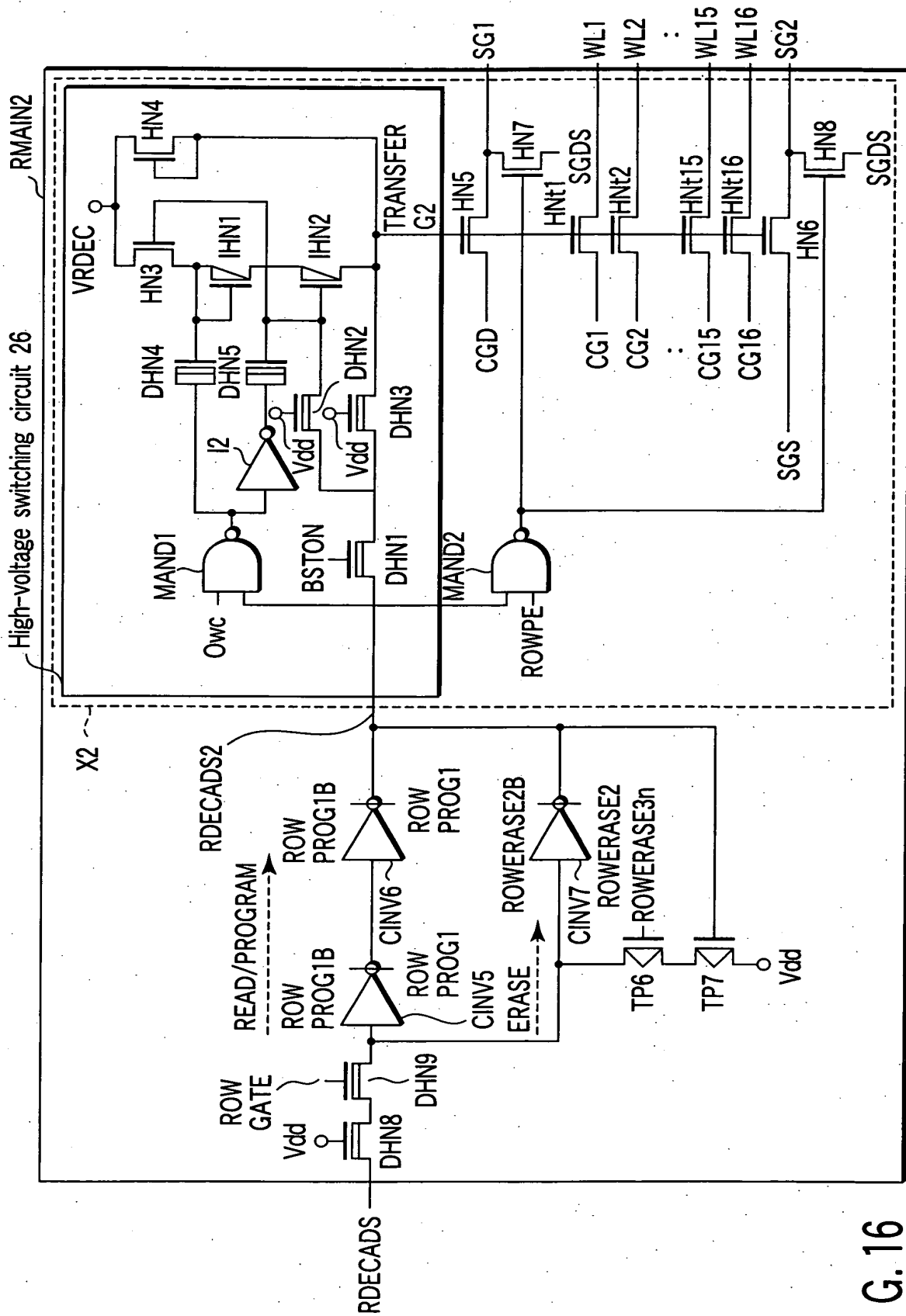


FIG.16

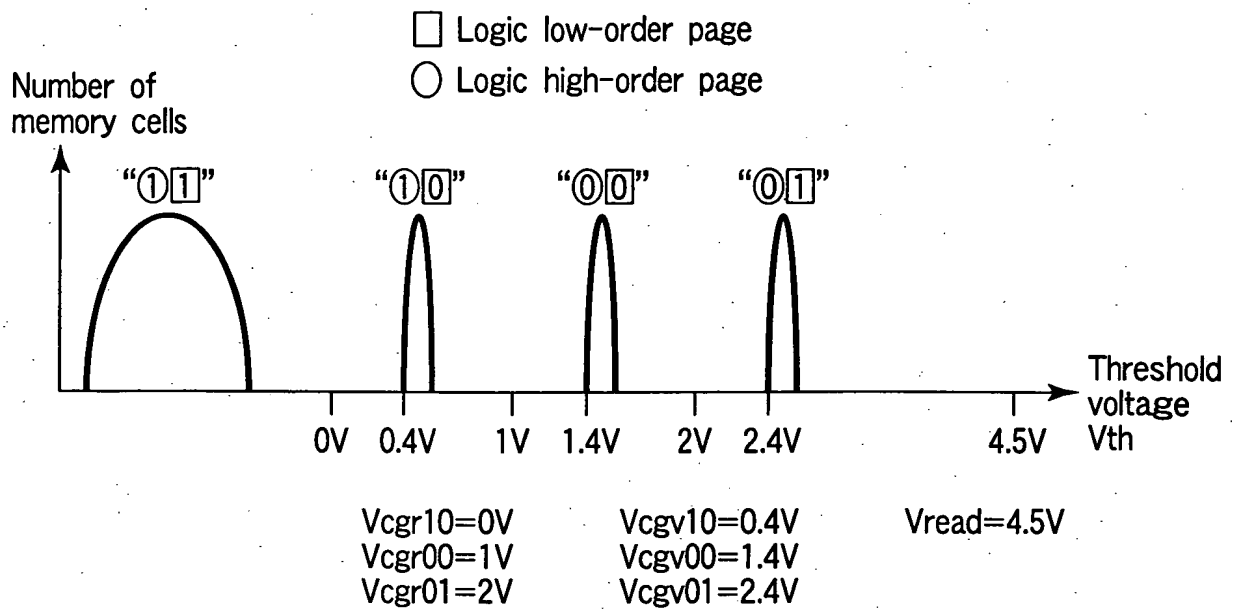


FIG. 17

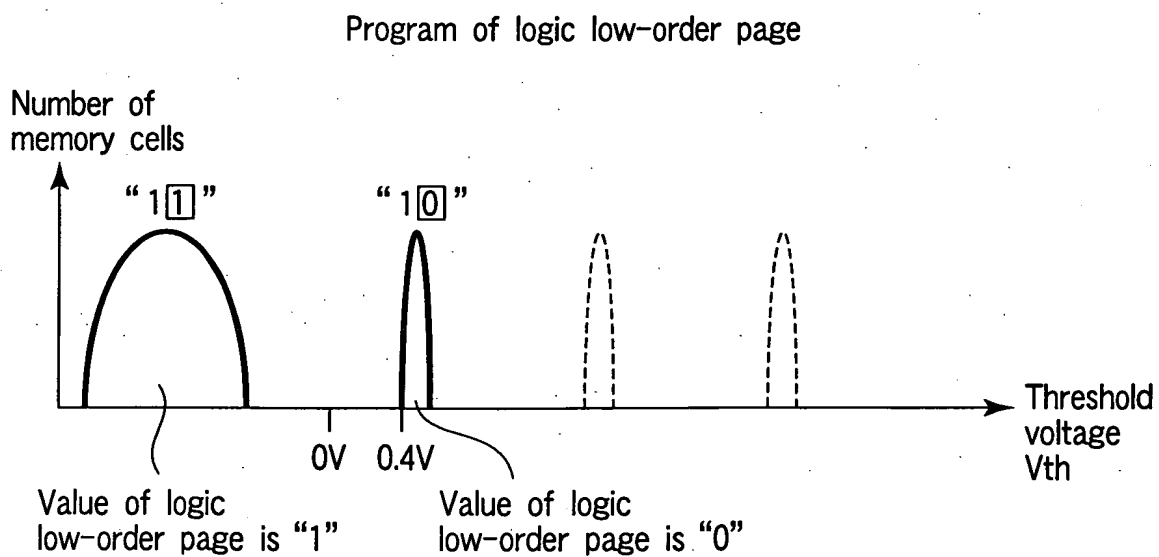


FIG. 18

Program of logic high-order page

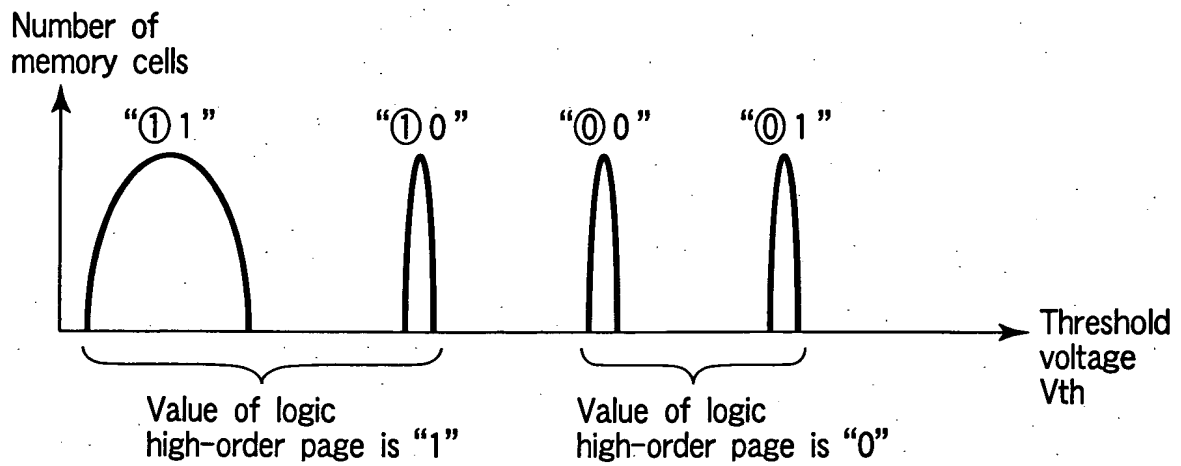


FIG. 19

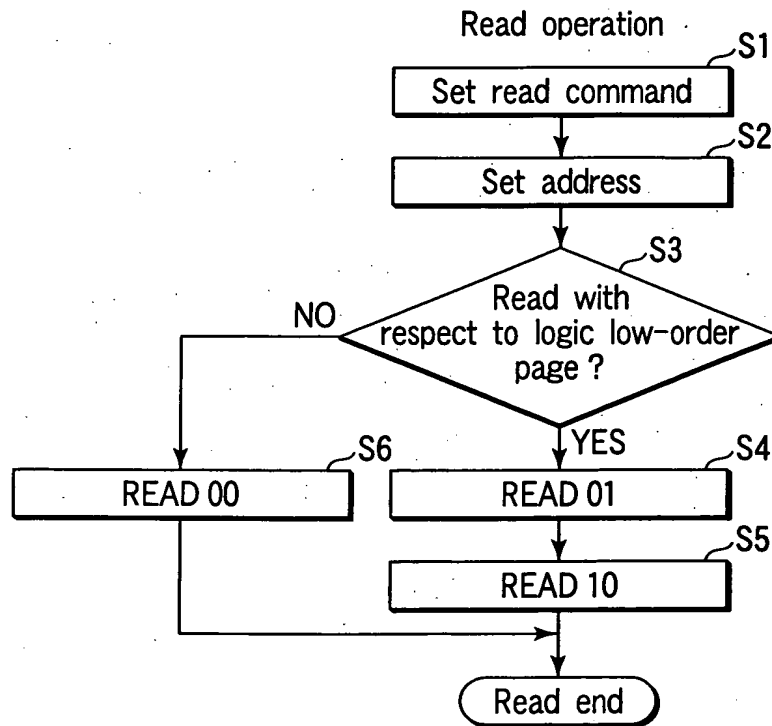


FIG. 20



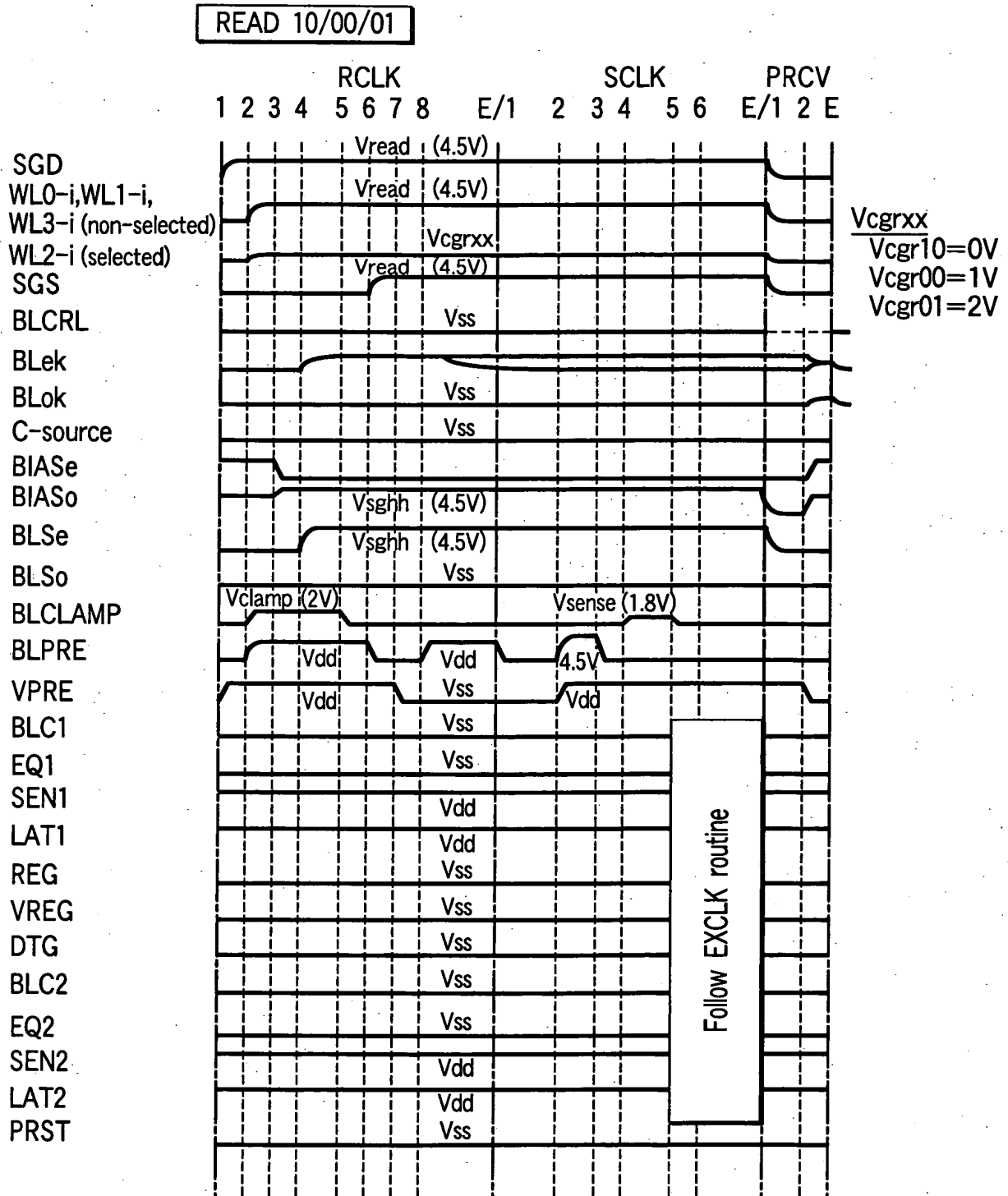
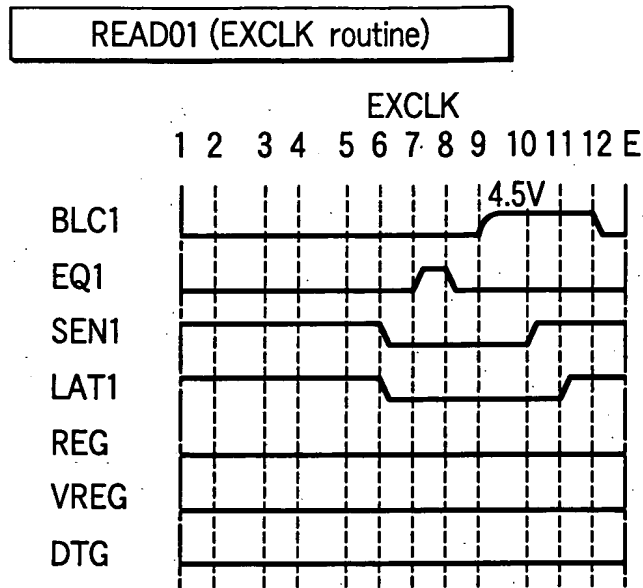
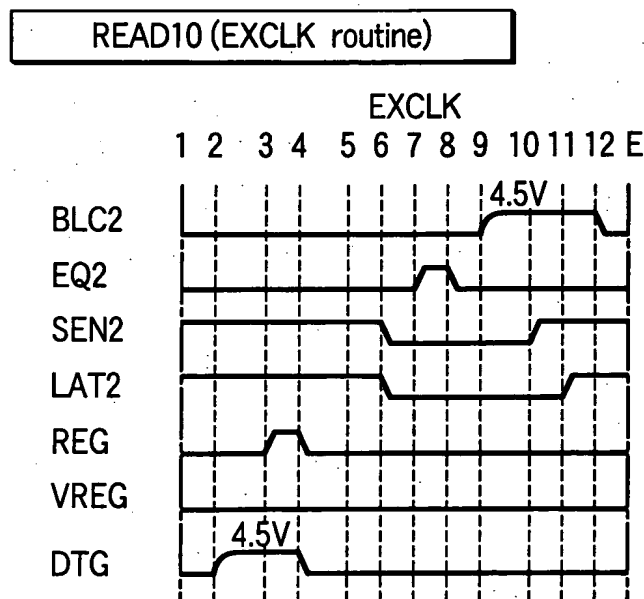


FIG. 21



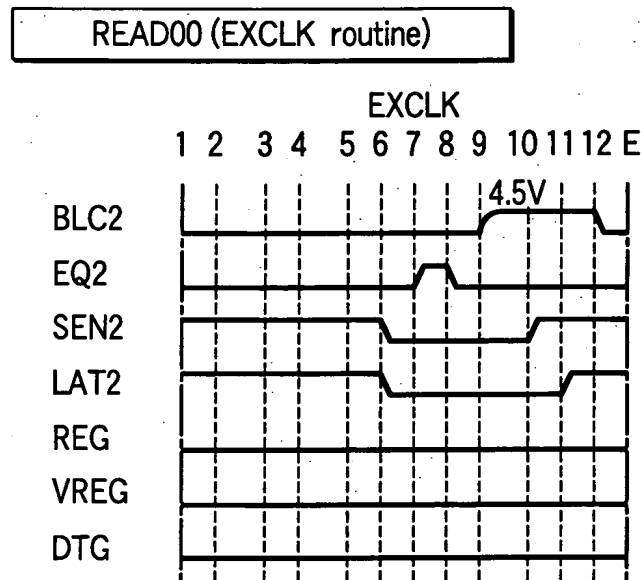
No change in signals other than shown signals

**FIG. 22**



No change in signals other than shown signals

**FIG. 23**



No change in signals other than shown signals

FIG. 24

Read of logic low-order page data

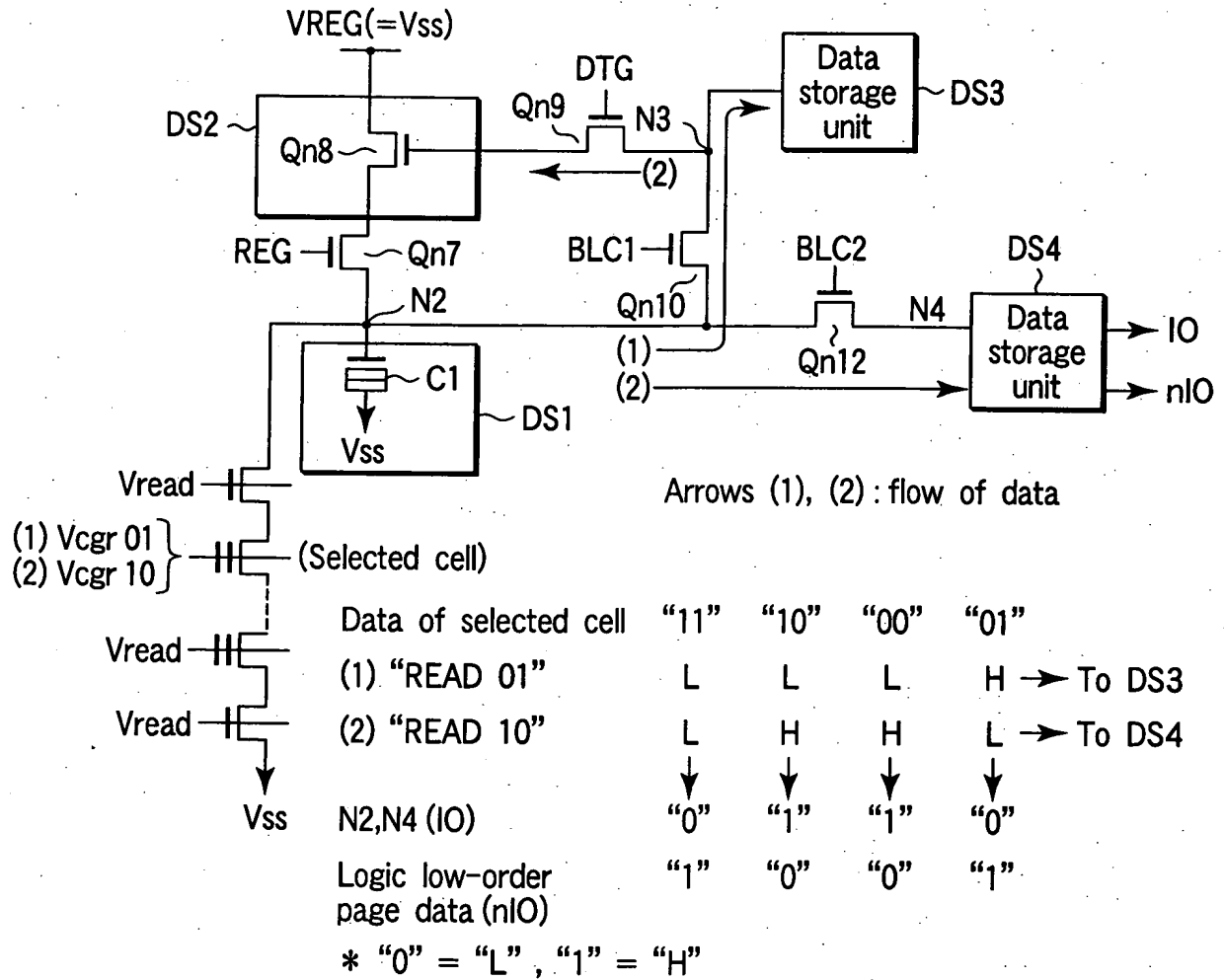


FIG. 25

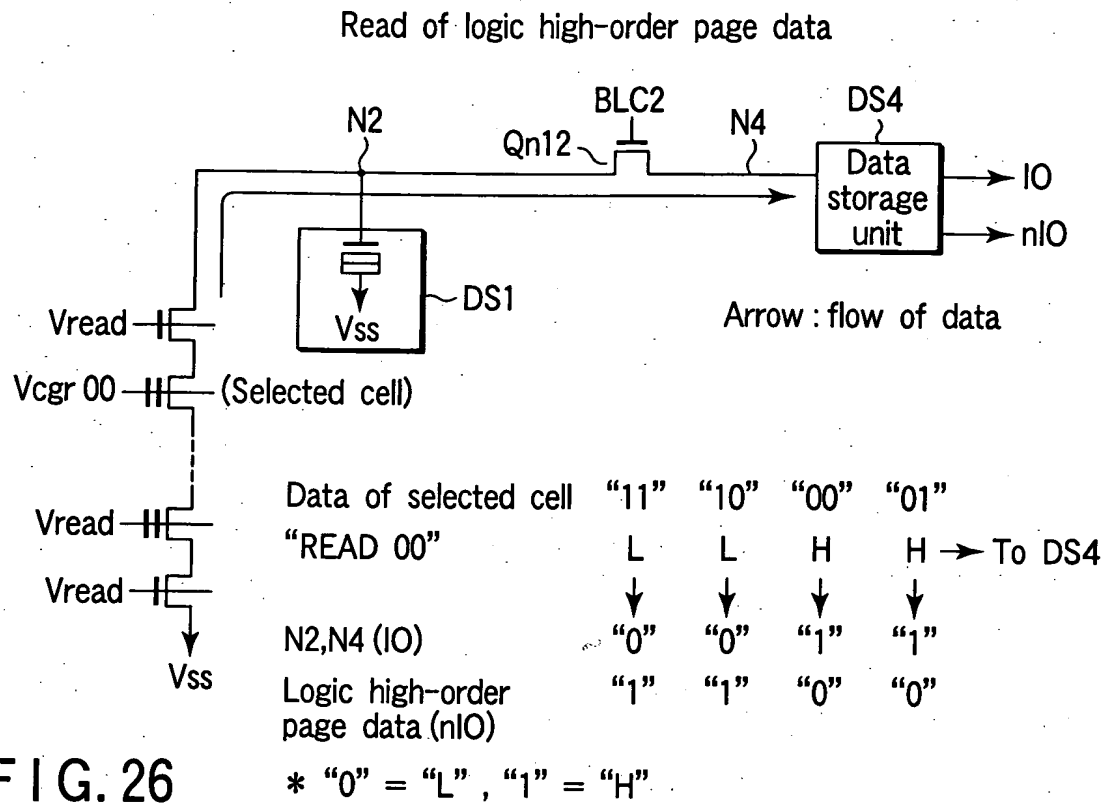


FIG. 26

Program operation 1 (Pass Write)

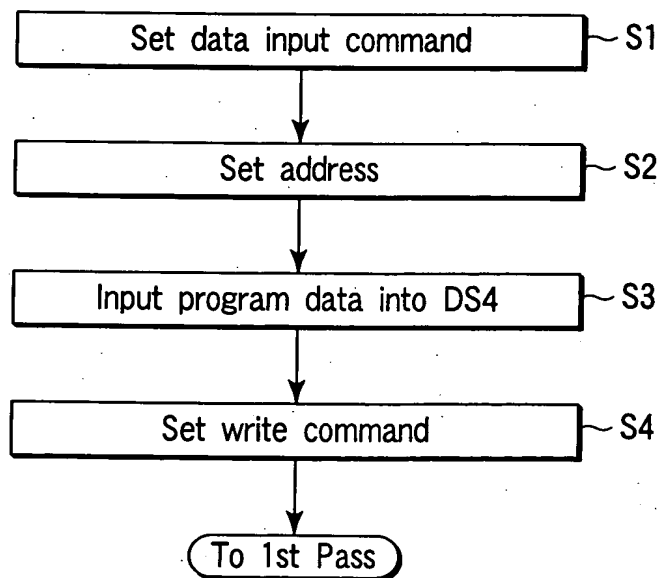


FIG. 27

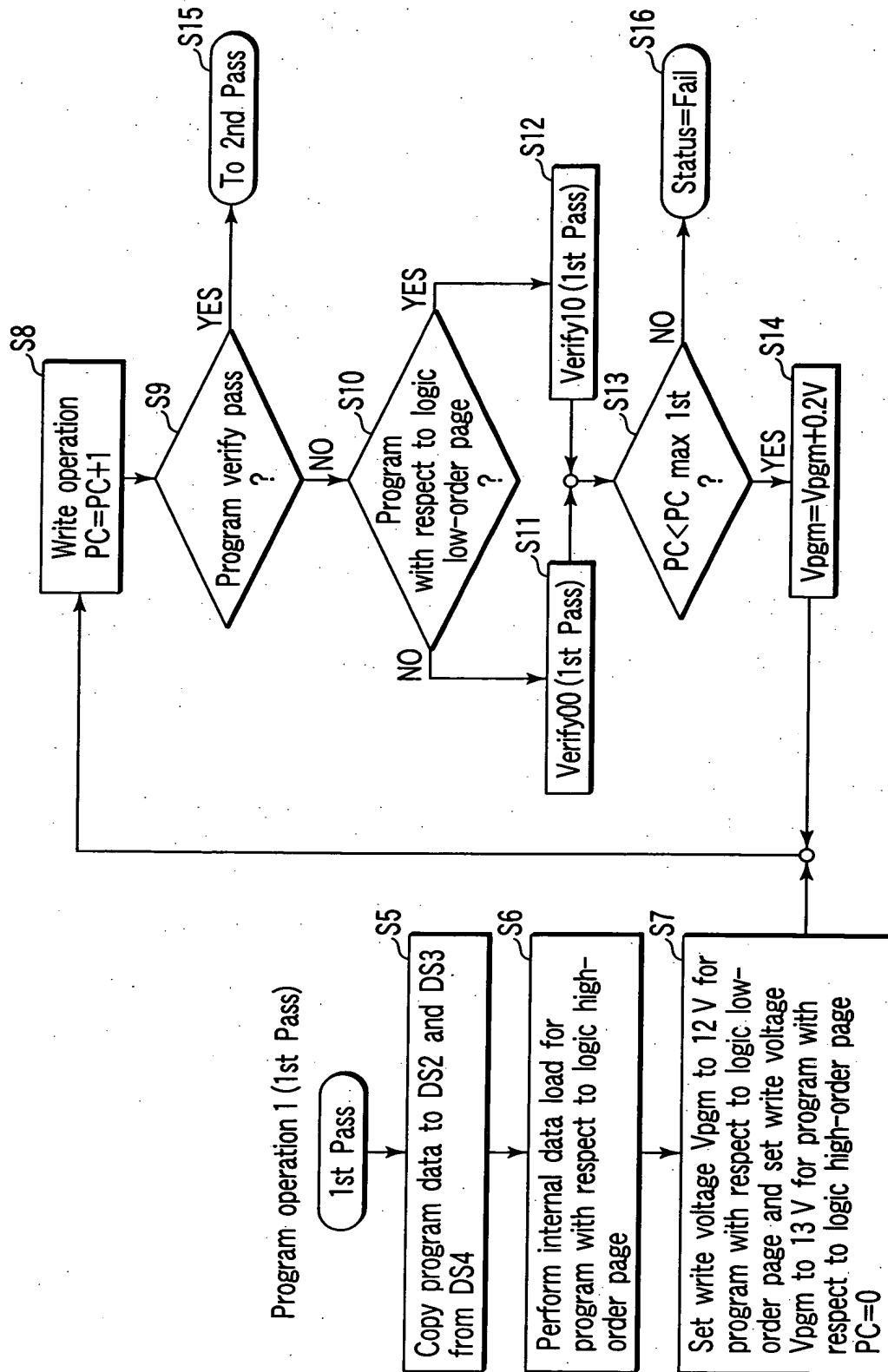


FIG. 28

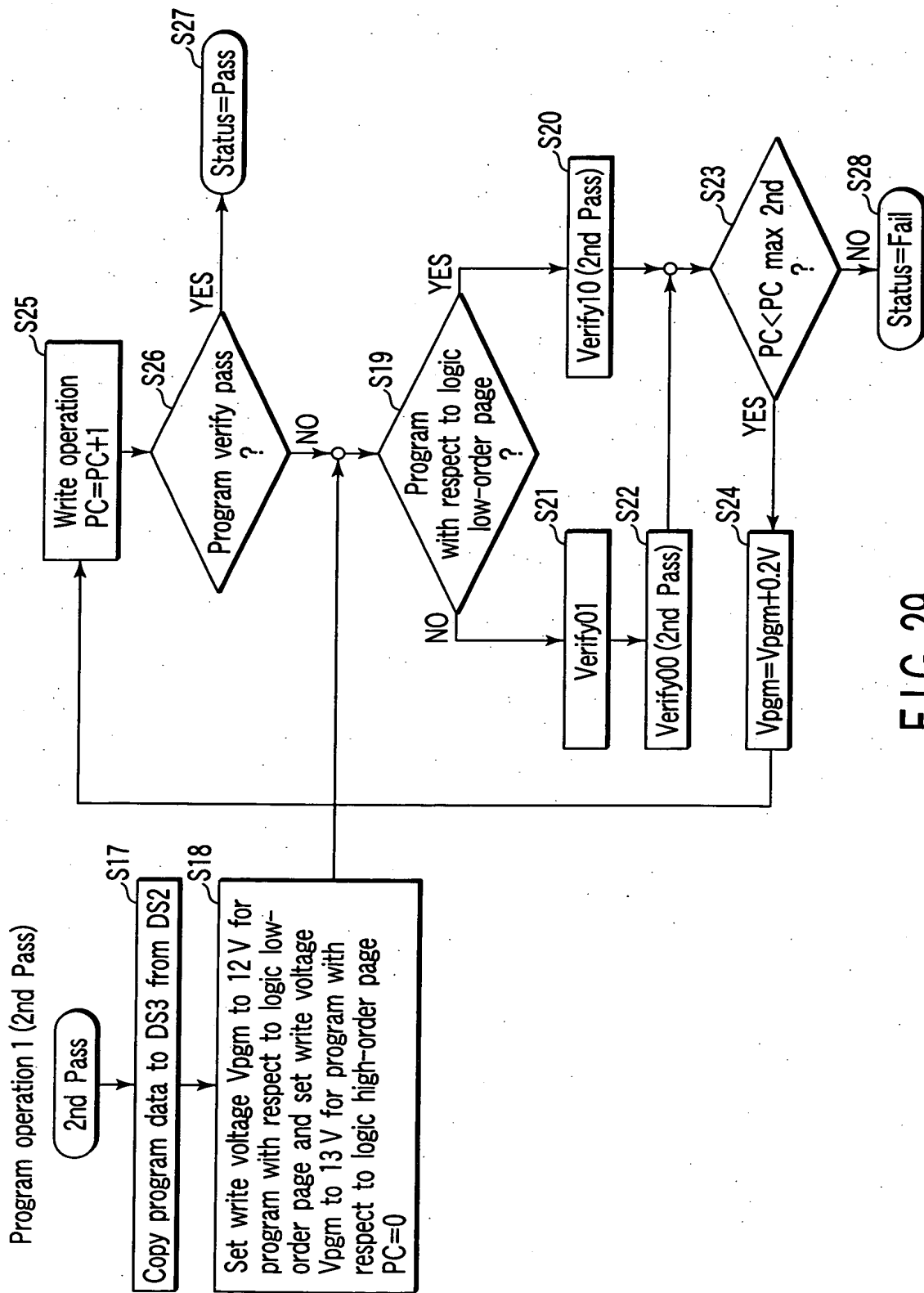


FIG. 29

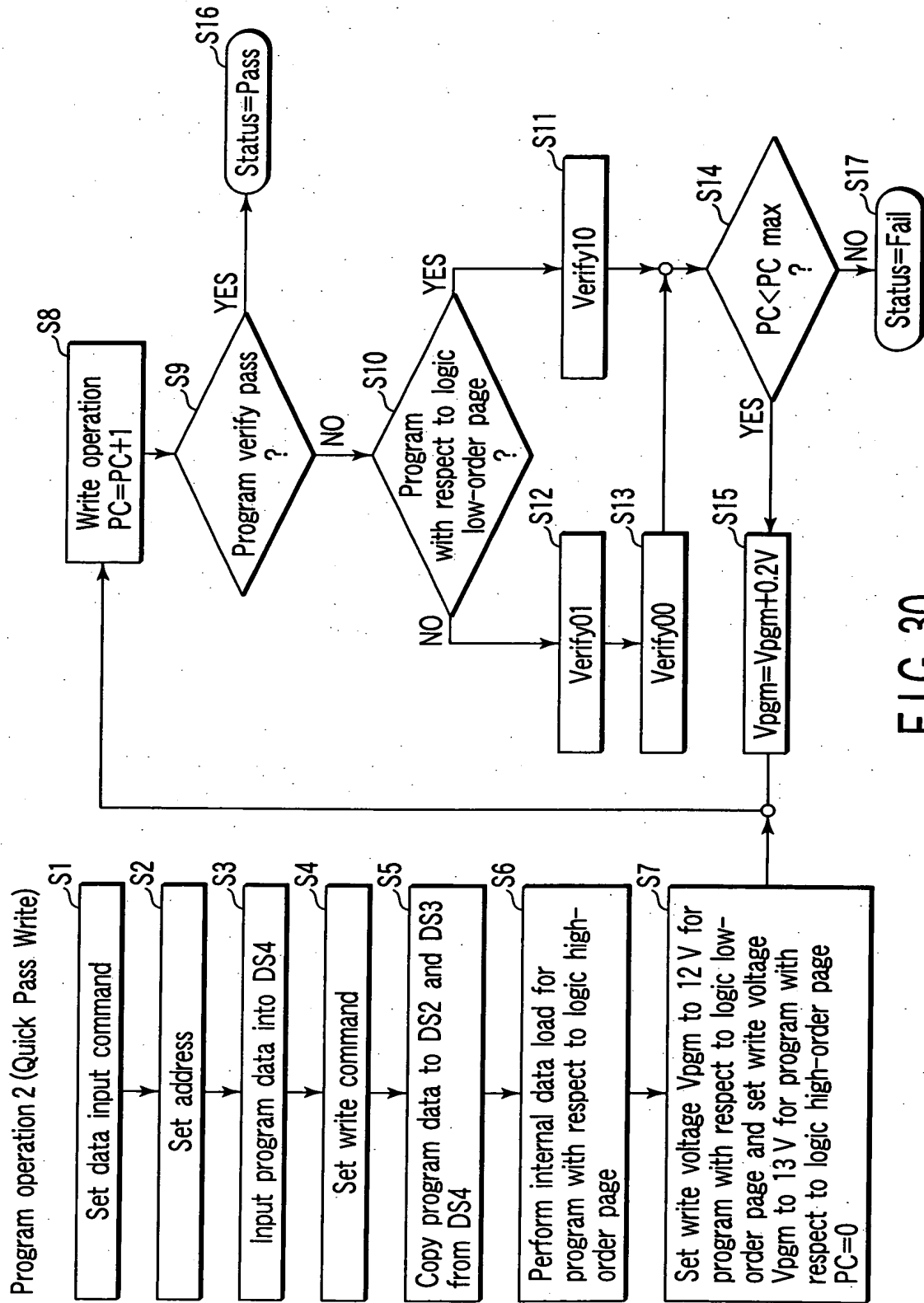


FIG. 30



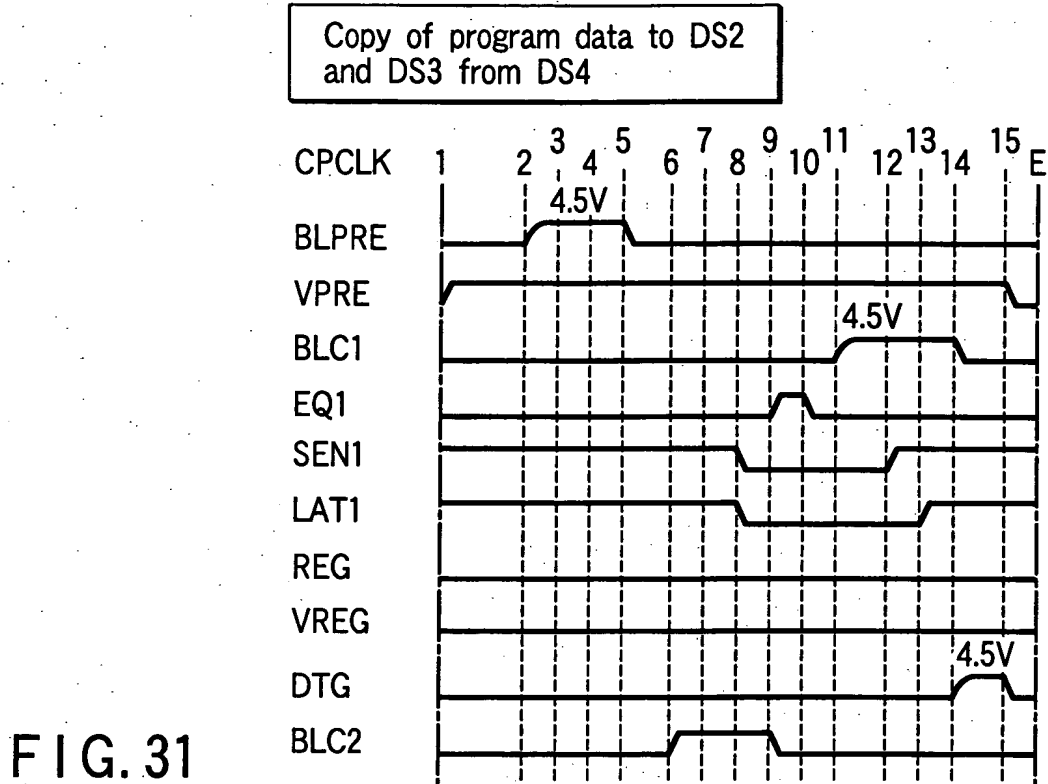


FIG. 31

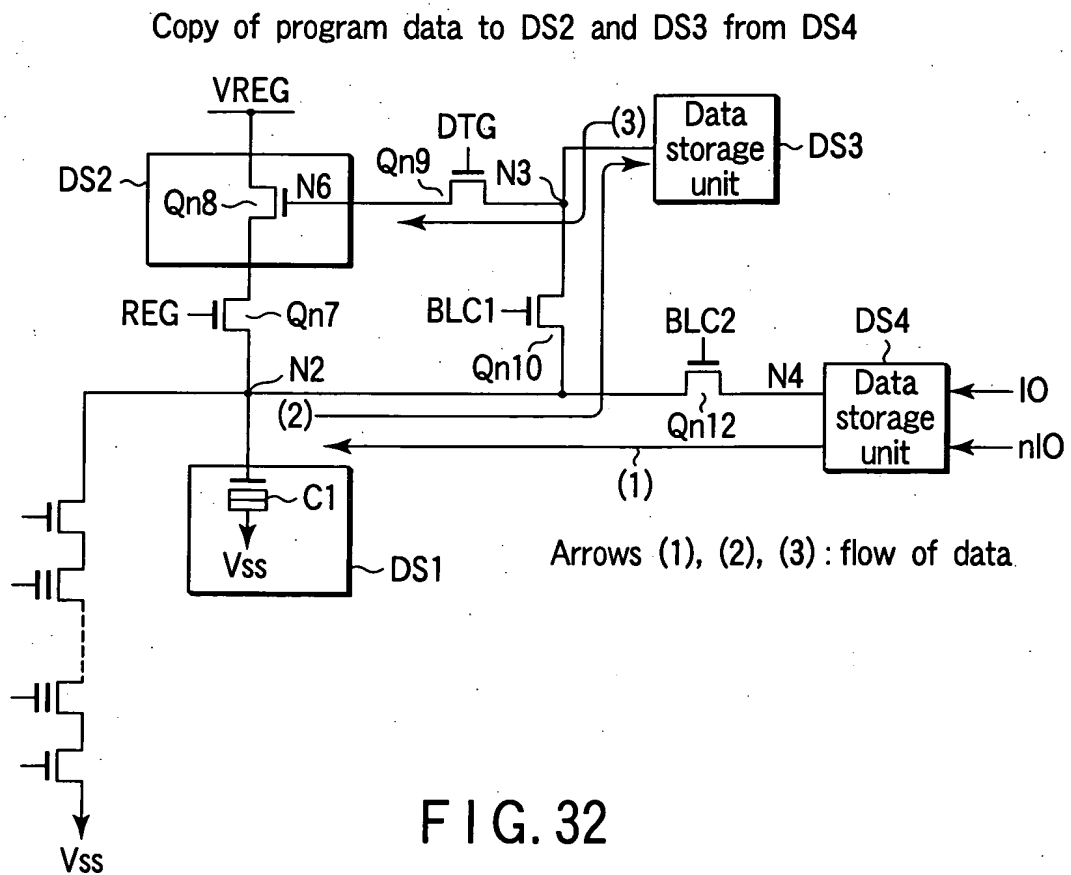


FIG. 32

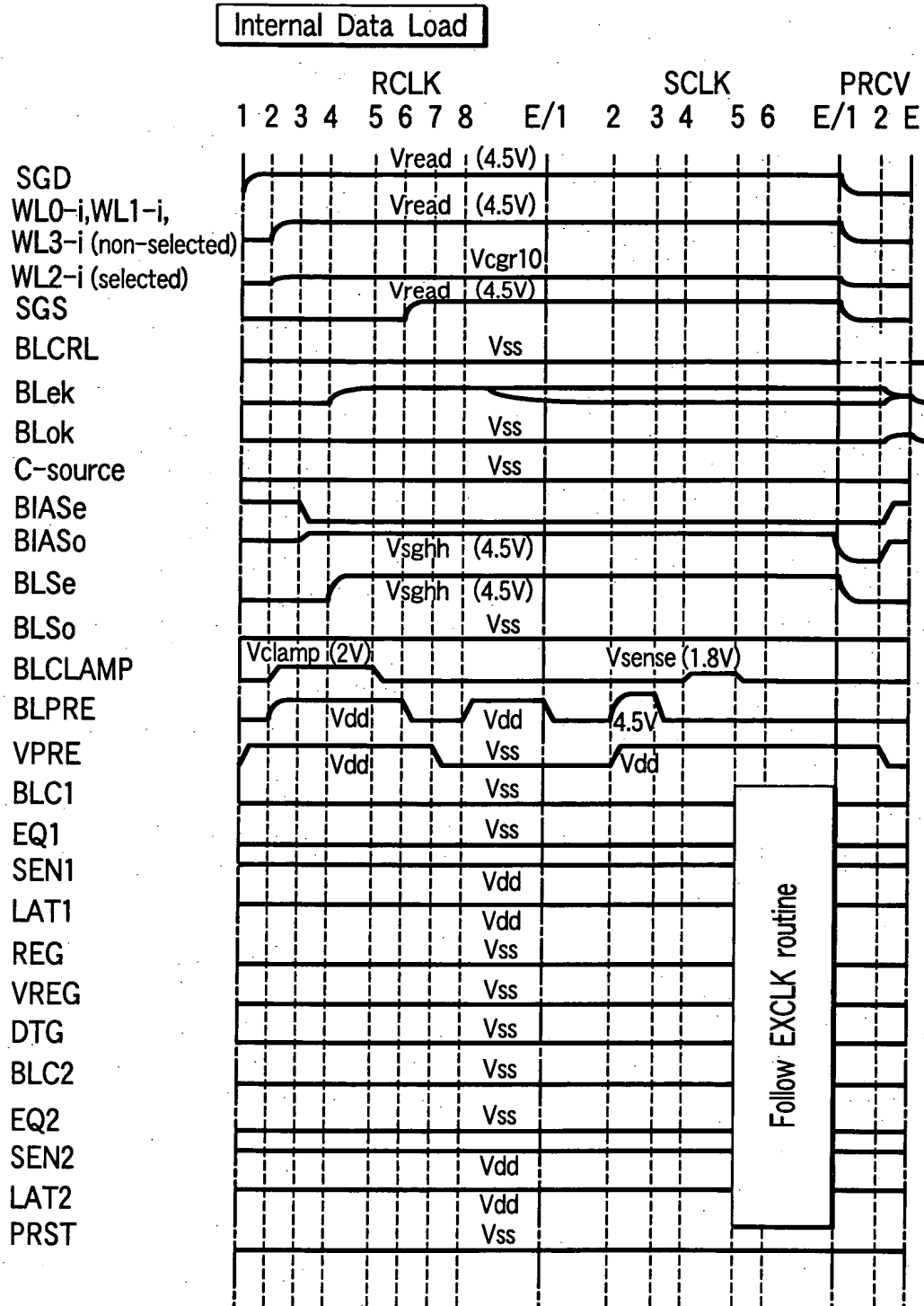
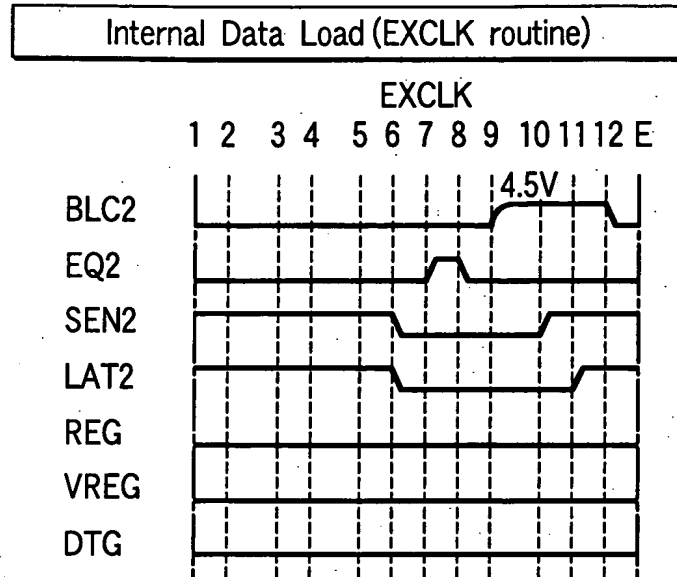
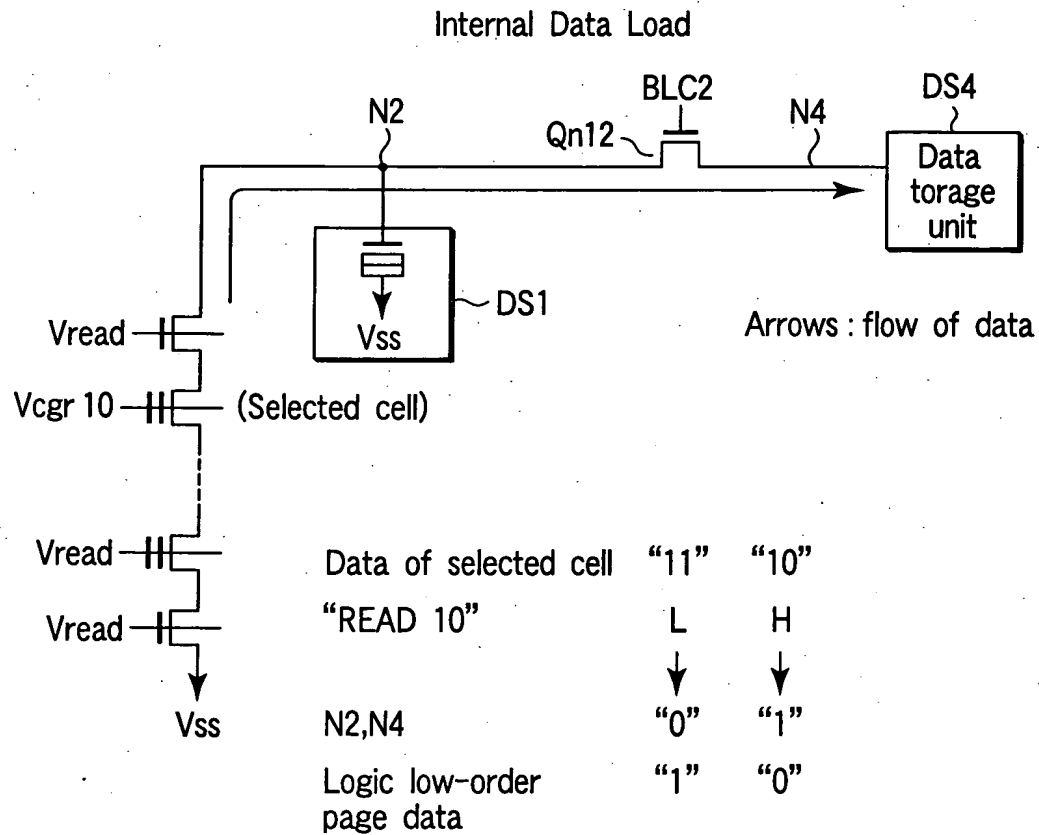


FIG. 33



**FIG. 34** No change in signals other than shown signals



**FIG. 35**

\* "0" = "L" , "1" = "H"

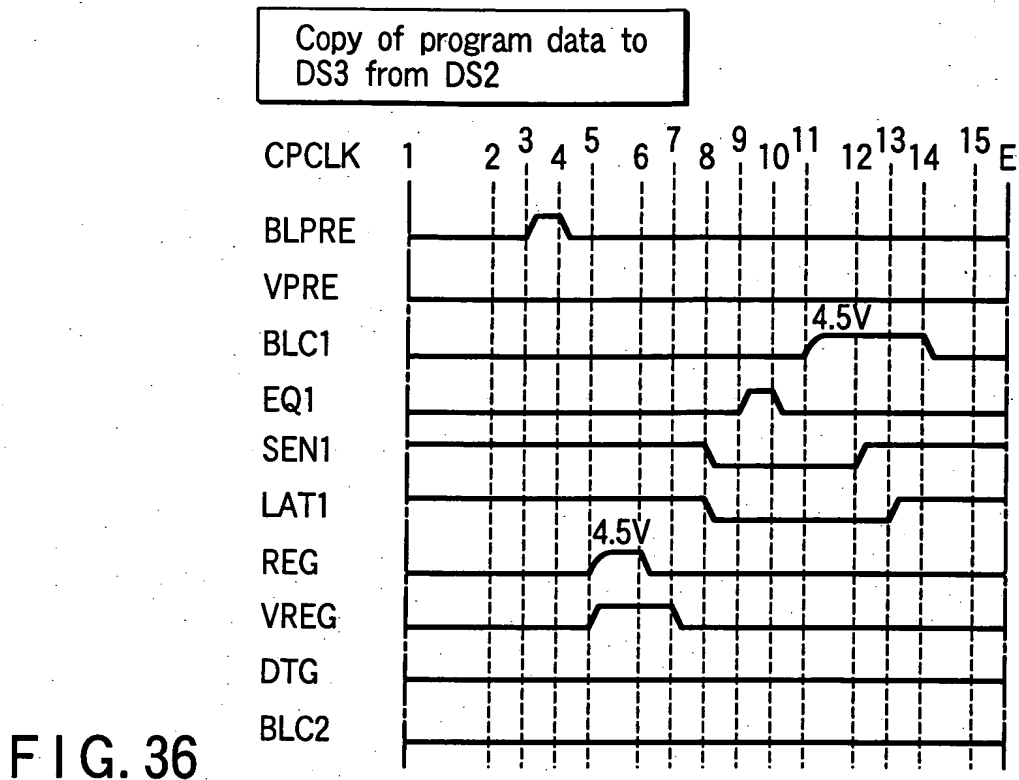


FIG. 36

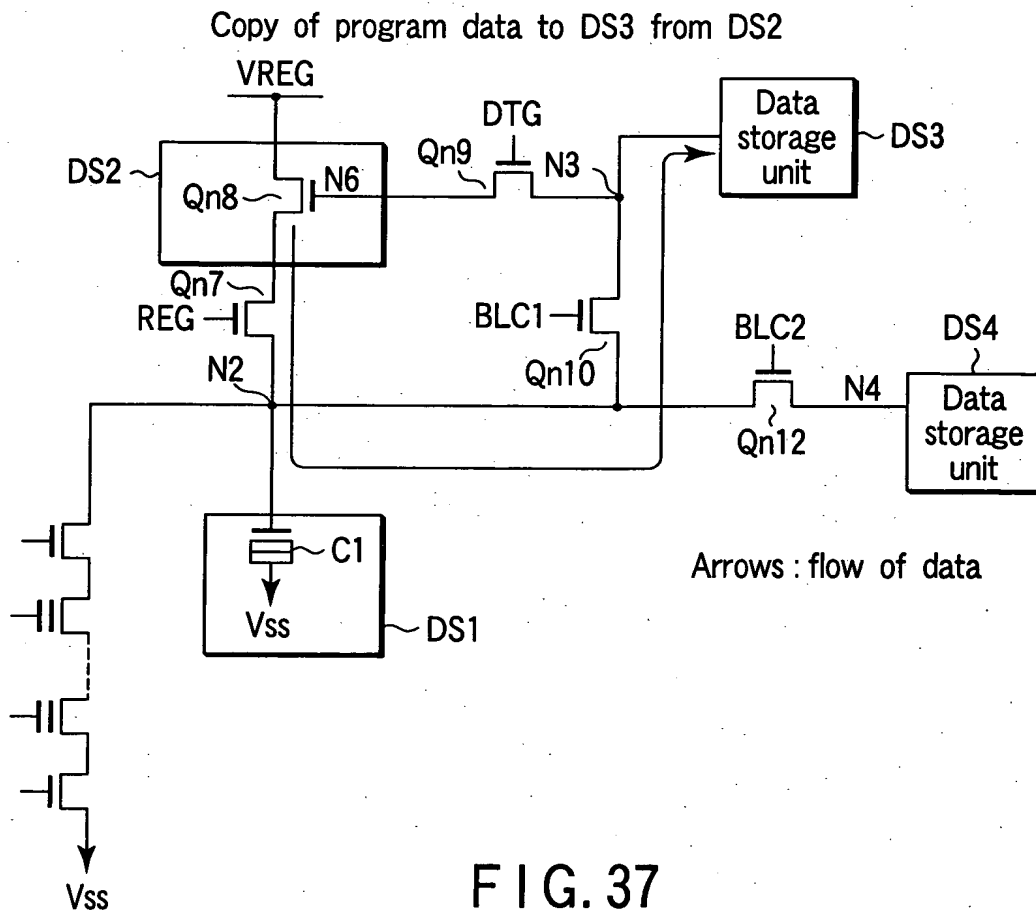


FIG. 37

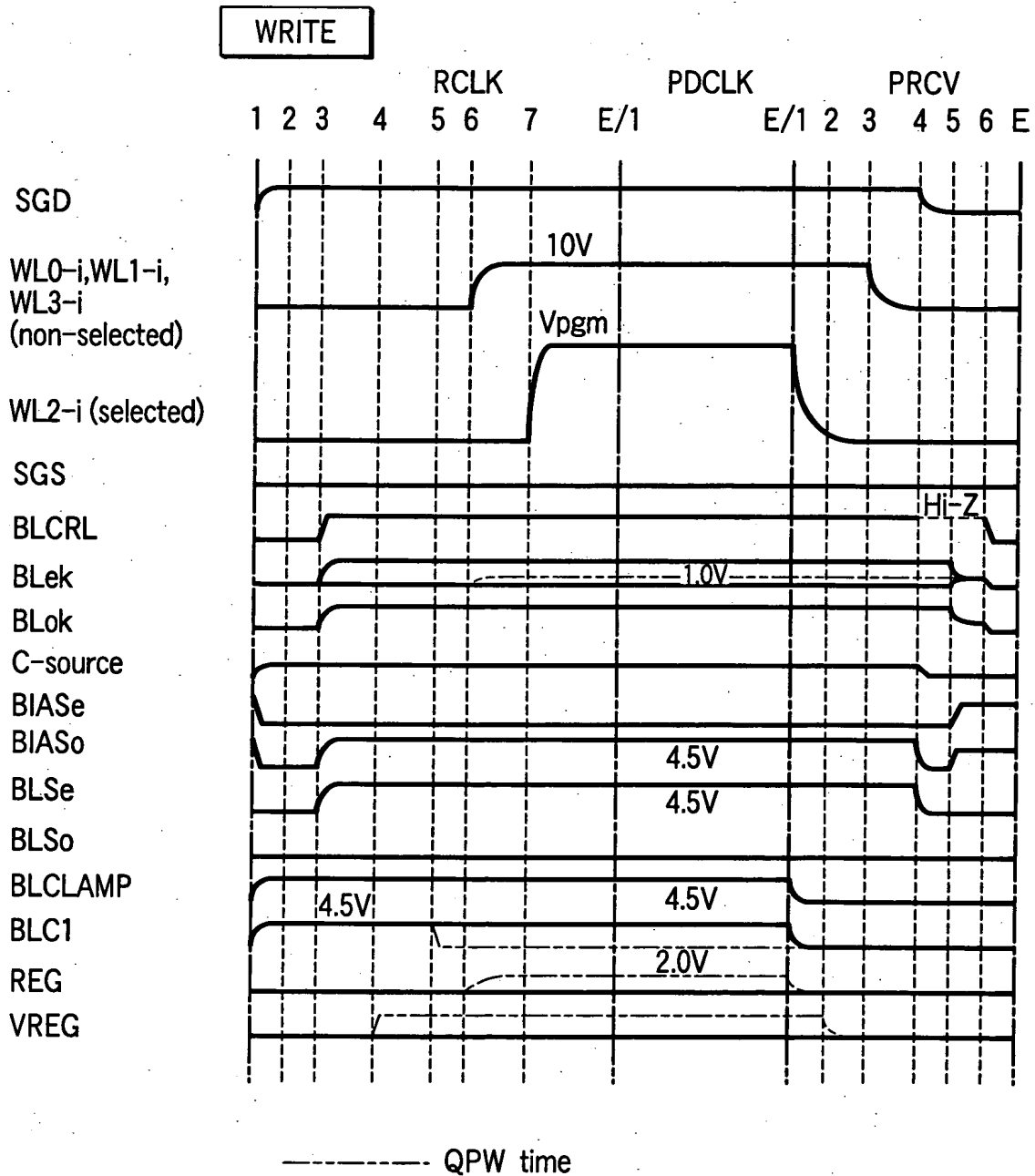


FIG. 38

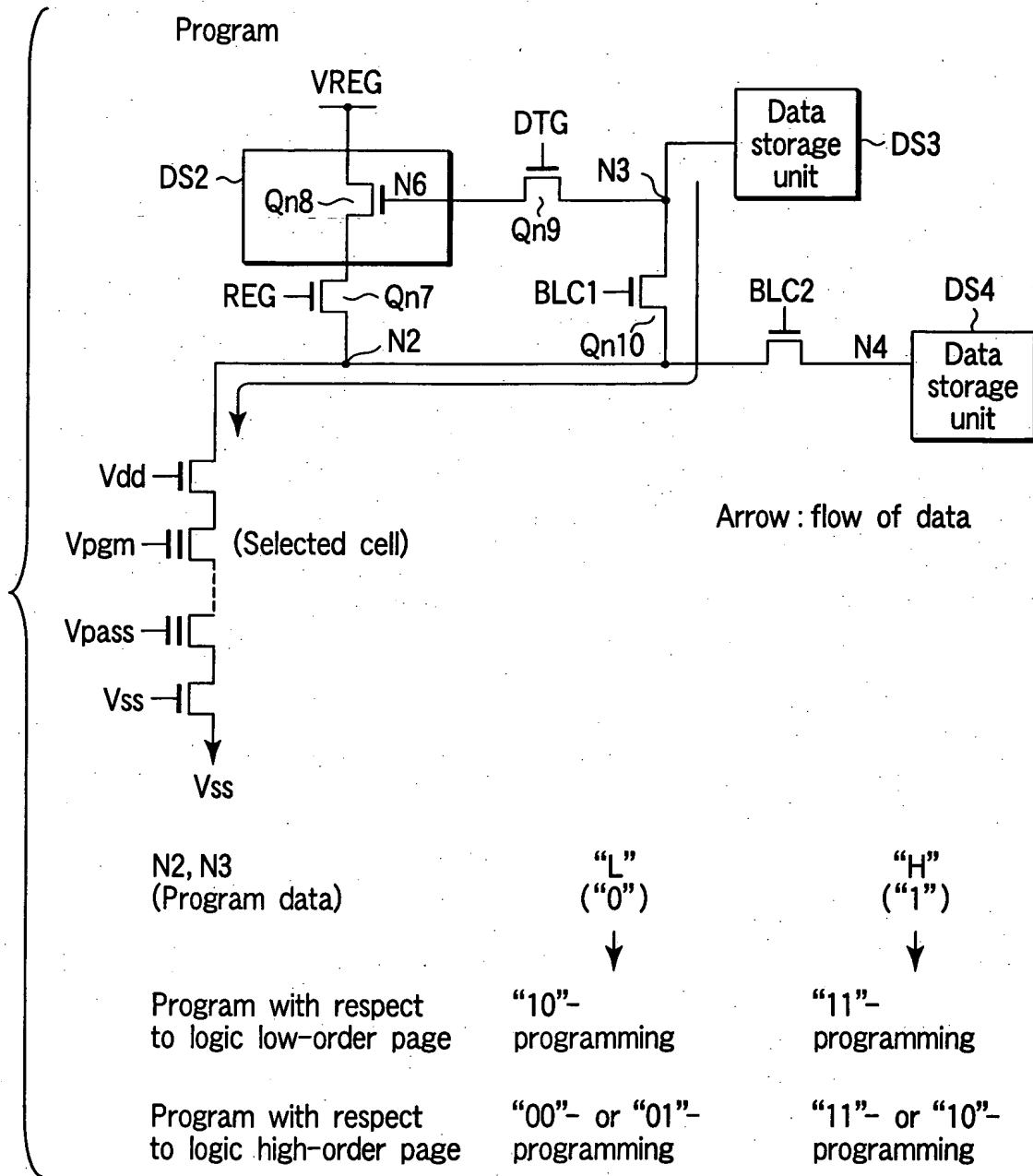


FIG. 39

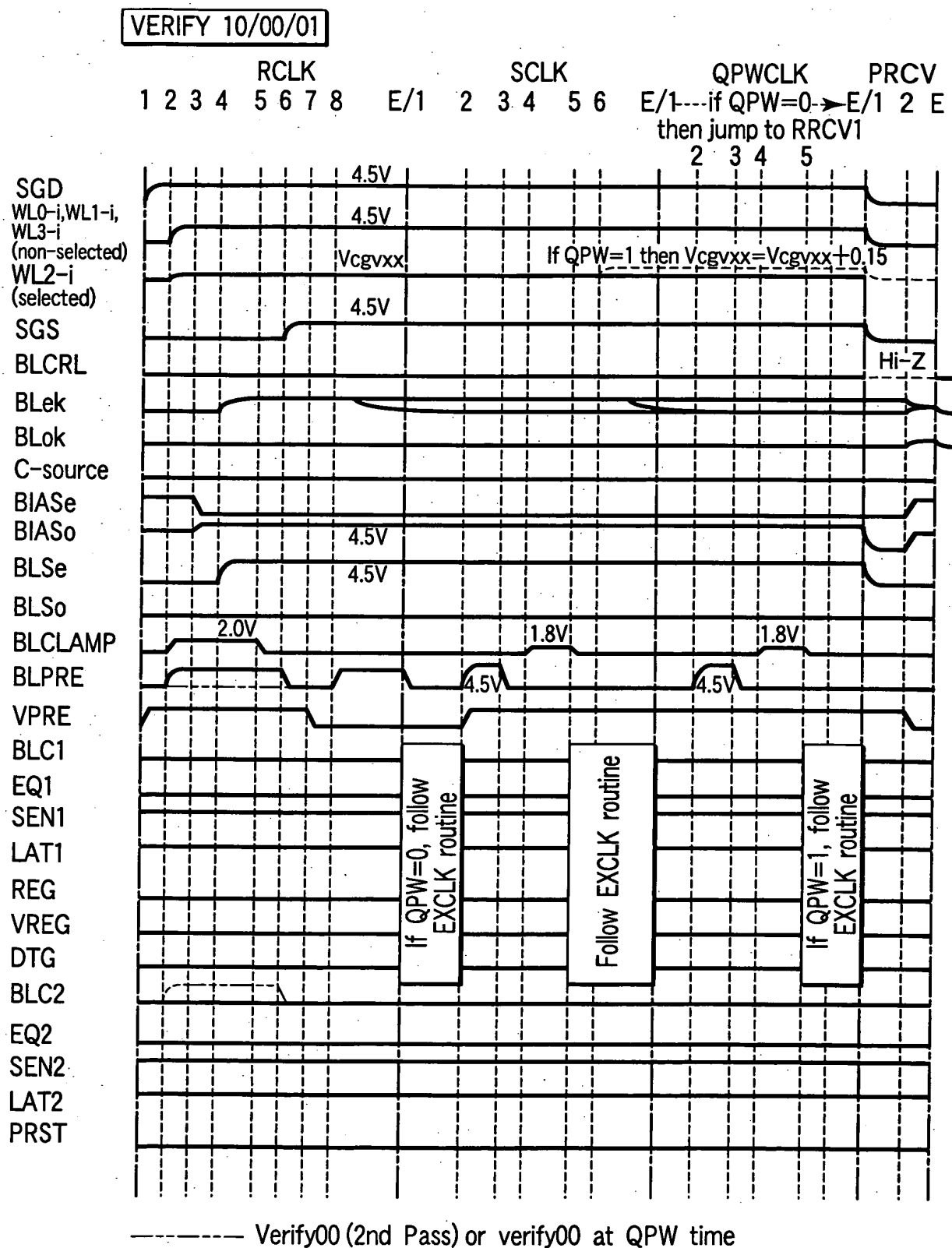


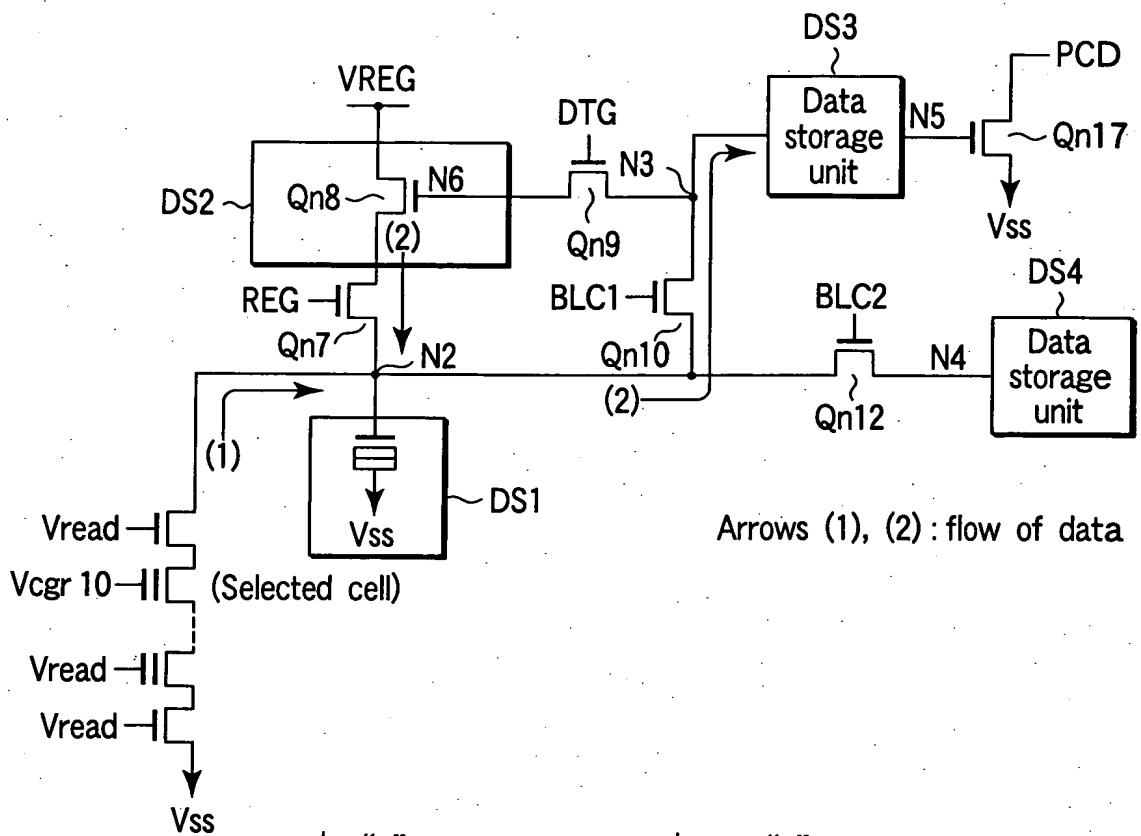
FIG. 40



FIG. 41



Program with respect to logic low-order page  
"VERIFY 10" + "COMPLETION DETECTION"



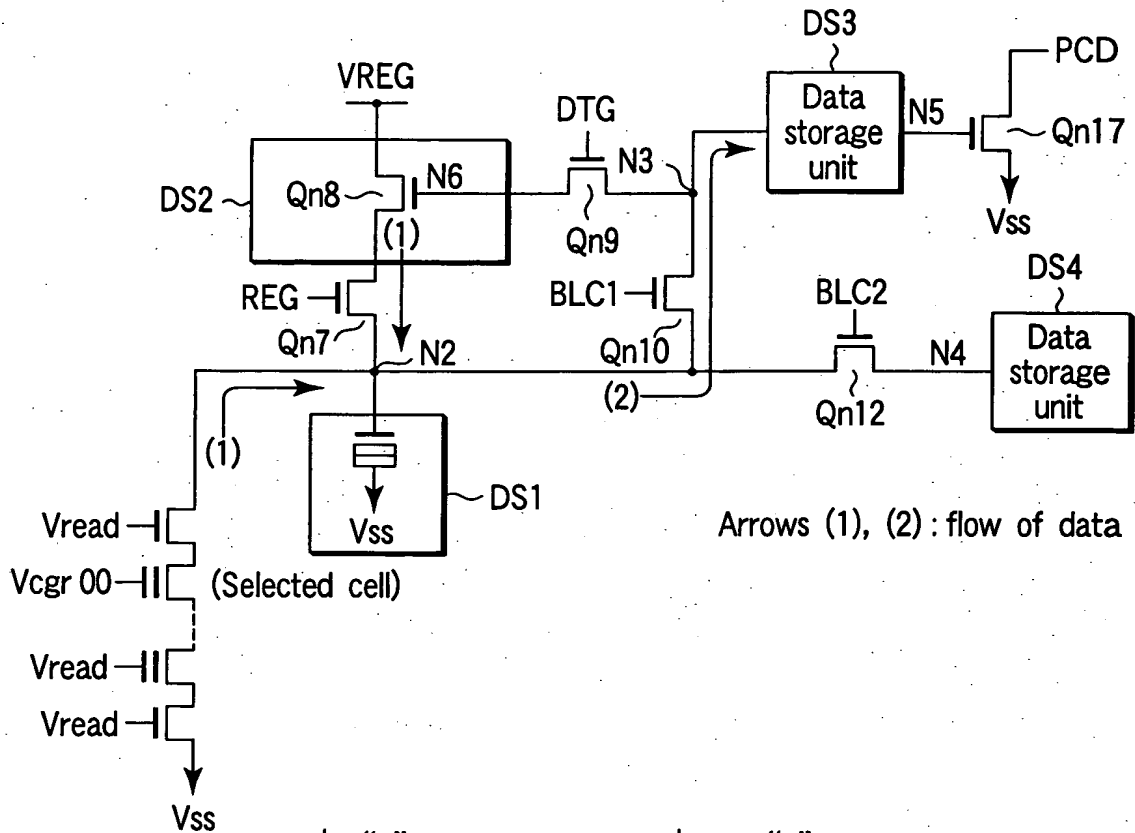
Arrows (1), (2) : flow of data

	"1"-programming		"0"-programming	
Data of selected cell (present state)	"11"		"11"	"10"
(1) DS1(N2)	"L" ("0")	⇒ "H" ("1")	"L" ("0")	"H" ("1")
(1) DS2(N6) Program data	"H" ("1")	※ Forcibly set DS1 to "H"	"L" ("0")	"L" ("0")
(2) DS3(N3)	"H" ("1")		"L" ("0")	"H" ("1")
N5	"L" program completed		"H" program uncompleted	"L" program completed

※ "Verify 10" includes "verify 10 (1st Pass)" in Write Pass, "Verify 10 (2nd Pass)" and "Verify 10" in Qwp

FIG. 42

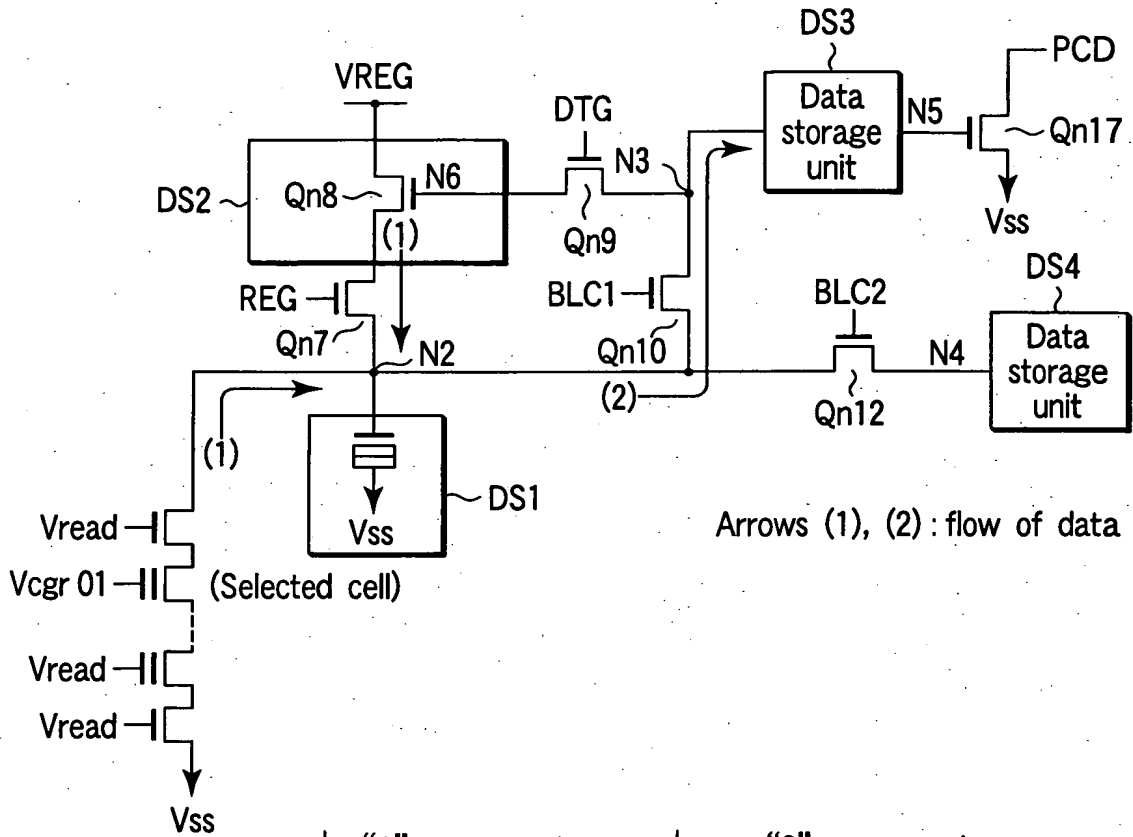
Program with respect to logic high-order page  
"VERIFY 00 (1st Pass)" + "COMPLETION DETECTION"



	"1"-programming		"0"-programming	
Data of selected cell (present state)	"11" or "10"		"11" or "10"	"00"
(1) DS1(N2)	"L" ("0")	⇒ "H" ("1")	"L" ("0")	"H" ("1")
(1) DS2(N6) Program data	"H" ("1")	※ Forcibly set DS1 to "H"	"L" ("0")	"L" ("0")
(2) DS3(N3)	"H" ("1")		"L" ("0")	"H" ("1")
N5	"L" program completed		"H" program uncompleted	"L" program completed

FIG. 43

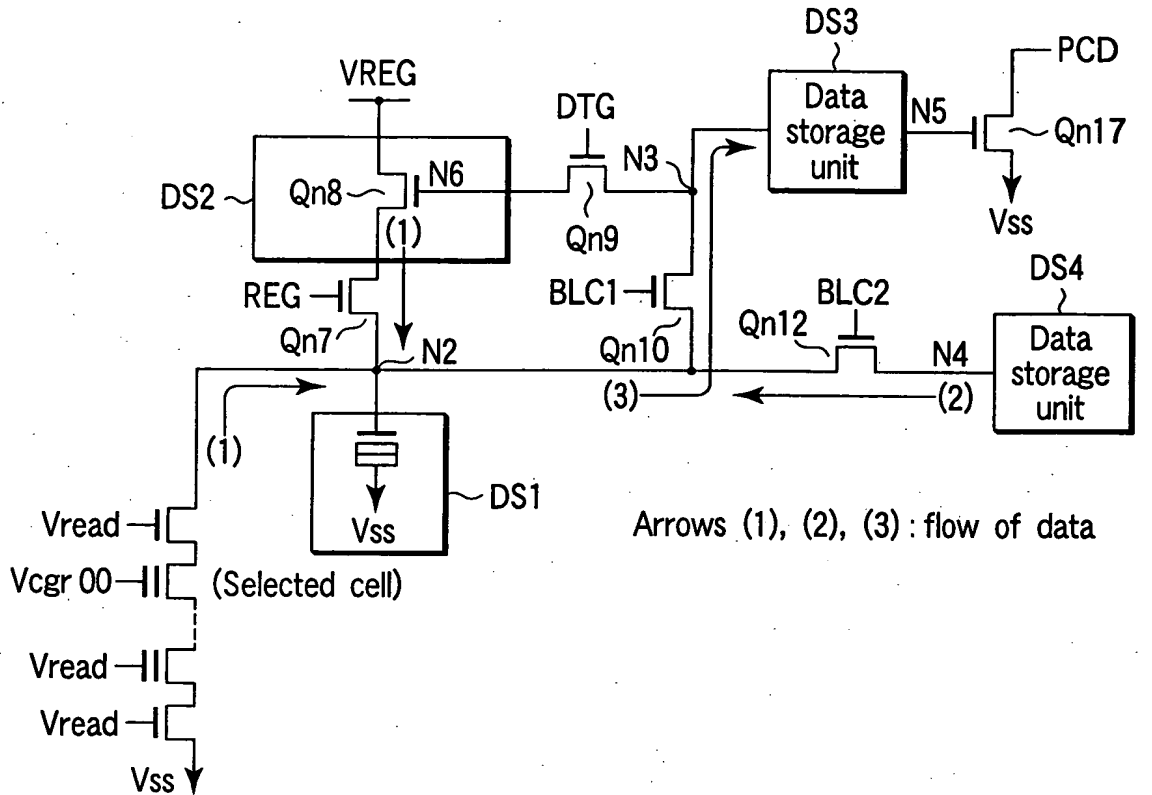
Program with respect to logic high-order page  
"VERIFY 01" + "COMPLETION DETECTION"



	"1"-programming		"0"-programming	
Data of selected cell (present state)	"11" or "10"		"11" or "10" or "00"	"01"
(1) DS1(N2)	"L" ("0")	⇒	"L" ("0")	"H" ("1")
(1) DS2(N6) Program data	"H" ("1")	※ Forcibly set DS1 to "H"	"L" ("0")	"L" ("0")
(2) DS3(N3)	"H" ("1")		"L" ("0")	"H" ("1")
N5	"L"		"H"	"L"
	program completed		program uncompleted	program completed

FIG. 44

Program with respect to logic high-order page  
"VERIFY 00 (2nd Pass)" + "COMPLETION DETECTION"



	"1"-programming		"0"-programming	
Data of selected cell (present state)	"11" or "10"		"11" or "10" or "00"	
(1) DS1(N2)	"L" ("0")	⇒ "H" ("1")	"L" ("0")	"H" ("1")
(2) DS2(N6) Program data	"H" ("1")	※Forcibly set DS1 to "H"	"L" ("0")	"L" ("0")
(2) Logic low-order page data (N4)			"0" ("H")	"1" ("L")
(2) DS1(N2)			"00"-programming "H" ("1")	※Forcibly set DS1 to "L" "01"-programming "H" ("1") ⇒ "L" ("0")
(3) DS3(N3)	"H" ("1")		"L" ("0")	"H" ("1")
N5	"L"		"H"	"L"
	program completed		program uncompleted	program completed
				program uncompleted

FIG. 45